



FEATURES

- Meets the Requirements of ISO11898-2
- Up to 5.0 kV_{rms} Insulation voltage
- VDD1 supply voltage: 2.5V to 5.5V
- Bus side power supply voltage: 4.75V to 5.25V
- Low-EMI 5Mbps Data Rate
- High CMTI: $\pm 80\text{kV}/\mu\text{s}$
- High system level EMC performance:
Bus Pins meet IEC61000-4-2 $\pm 8\text{kV}$ ESD
- Driver (TXD) Dominant Time-out Function
- Low loop delay: 130ns typical, 220ns maximum
- Operation temperature: $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- RoHS-compliant, Wide-body SOIC-16 package
- Safety-related certifications:
– $1200\text{V}_{\text{peak}}$ V_{IORM} per DIN VDE V0884-17: 2021-10
– 5.0kV_{rms} isolation for 1 minute per UL 1577
– CQC and CB approvals

APPLICATIONS

- Isolated CAN Communication
- Industrial automation, control, and drive systems
- Medical systems
- Transportation
- HVAC systems and building automation

GENERAL DESCRIPTION

The **Pai845x** is a 2PaiSemi isolated CAN Transceivers product family that provide outstanding performance characteristics by using 2PaiSemi **iDivider**® technology.

Intelligent voltage divider technology (**iDivider**® technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The Pai8451 is an isolated CAN Transceiver. All the devices are certified with 5kV_{rms} isolation voltage per UL 1577 and meets the specifications of the ISO11898-2 standard.

Combined with isolated power supplies, Pai8451 prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

As a CAN transceiver, Pai8451 provides differential-signal transmit capability to the bus and differential-signal receive capability to a CAN controller at signaling rates up to 5Mbps. Pai8451 is designed for harsh-environment operation, and it features crosswire, overvoltage, and loss of ground protection from -40 V to $+40\text{ V}$ and overtemperature shutdown, as well as -12 V to 12 V common-mode range.

FUNCTIONAL BLOCK DIAGRAMS

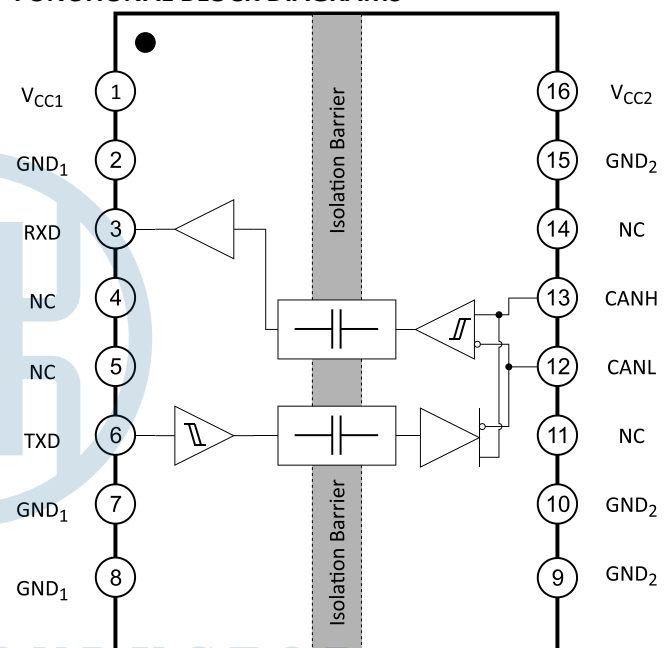


Figure 1. Pai8451 functional block diagram

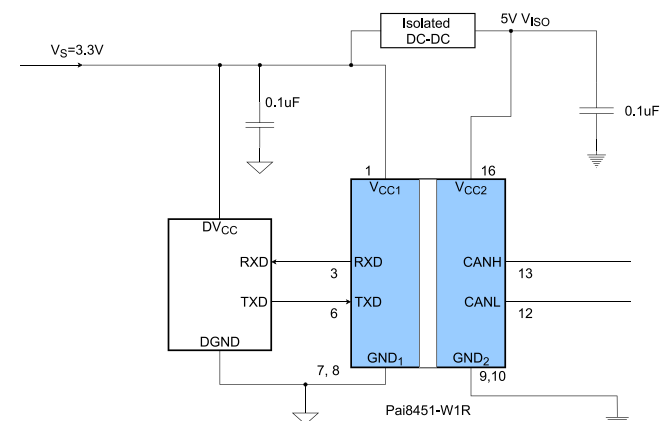


Figure 2. Pai8451 Typical Application Circuit

Rev.1.0

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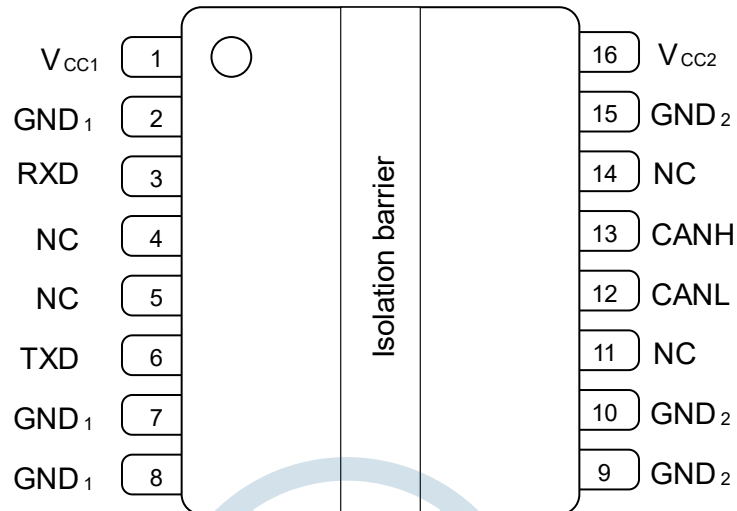
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PIN CONFIGURATIONS AND FUNCTIONS

WB SOIC-16 Package

Isolated CAN Transceiver

Top View



Not to scale

Figure 3. Pai8451 Pin Configurations

Table 1. Pai8451-W1R Pin Function Descriptions

PIN NO.	PIN NAME	DESCRIPTION
1	V _{cc1}	Digital-side supply voltage (2.5 to 5.5 V)
2	GND ₁	Digital-side ground connection
3	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
4	NC	No connect
5	NC	No connect
6	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
7	GND ₁	Digital-side ground connection
8	GND ₁	Digital-side ground connection
9	GND ₂	Transceiver-side ground connection
10	GND ₂	Transceiver-side ground connection
11	NC	No connect
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	NC	No connect
15	GND ₂	Transceiver-side ground connection
16	V _{cc2}	Transceiver-side supply voltage (5 V)

SPECIFICATIONS

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

DESCRIPTION		MIN	MAX	UNIT
V _{CC1}	Supply voltage, side 1	-0.5	6	V
V _{CC2}	Supply voltage, side 2	-0.5	6	V
V _{IO}	Logic voltage level (TXD, RXD)	-0.5	V _{CC1} +0.5 ⁽³⁾	V
I _O	Output current on RXD pin	-15	15	mA
V _{CANH} & V _{CANL}	Voltage on bus pins (CANH, CANL w.r.t GND ₂)	-40	+40	V
T _J	Junction temperature	-40	150	°C
T _{STG}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND₁ or GND₂) and are peak voltage values.

(3) Maximum voltage must not exceed 6 V

ESD Rating

Table 3. Pai8451 ESD Ratings

DESCRIPTION			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Logic pins and GND ₁	±6000
			Bus pins and GND ₂	±6000
			All pins	±4000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1000

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operation Conditions

Table 4. Recommended Operating Conditions

DESCRIPTION		MIN	TYP	MAX	UNIT
V _{CC1}	Digital-side supply voltage	2.5		5.5	V
V _{CC2}	Transceiver-side supply voltage	4.75	5	5.25	V
V _{ib}	Bus Pin Stress Voltage	-12		12	V
V _{IH}	Input threshold high at TXD pin	0.7		1	xVDD
V _{IL}	Input threshold low at TXD pin	0		0.3	xVDD
V _{ID}	Differential input voltage	-7		7	V
I _{OH}	Driver high level output current	-70			mA
	Receiver high level output current	-5			mA
I _{OL}	Driver low level output current			70	mA
	Receiver low level output current			5	mA
T _A	Ambient temperature	-40		125	°C
T _J	Junction temperature	-40		150	°C
P _D	Total power dissipation			438	mW
P _{D1}	Power dissipation by Side-1			25	mW
P _{D2}	Power dissipation by Side-2			413	mW

Driver Truth Table

Table 5. Pai8451 Driver Truth Table

Input	Outputs		Driven Bus state
TXD	CANH	CANL	
L	H	L	Dominant
H	Z	Z	Recessive

(1) L=Logic Low, H= Logic High. X=H, L or floating, Z= High impedance.

Receiver Truth Table

Table 6. Pai8451 Receiver Truth Table

Device Mode	CAN Bus differential inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus state	RXD
Normal	$V_{ID} \geq 0.9V$	Dominant	L
	$0.5V < V_{ID} < 0.9V$	Indeterminate	Indeterminate
	$V_{ID} \leq 0.5V$	Recessive	H
	Open $V_{ID}=0V$	Open	H

(1) H = Logic high, L = Logic Low.

Function Table

Table 7. Pai8451 Device Truth Table

Driver			Receiver			
Inputs	Outputs		Bus state	Differential inputs	Output RXD	Bus state
TXD	CANH	CANL		$V_{ID}=CANH-CANL$		
L ⁽²⁾	H	L	Dominant	$V_{ID} \geq 0.9V$	L	Dominant
H	Z	Z	Recessive	$0.5V < V_{ID} < 0.9V$	Indeterminate	Indeterminate
Open	Z	Z	Recessive	$V_{ID} \leq 0.5V$	H	Recessive
X	Z	Z	Recessive	Open $V_{ID}=0V$	H	Open

(1) H = logic high, L = logic low.

(2) Logic low pulses to prevent dominant time-out.

Thermal Information

Table 8. Pai8451 WB SOIC-16 Thermal Information

PACKAGE THERMAL RATINGS		Rating	UNIT
$R_{\theta JA}$	Junction-to-Ambient thermal resistance	81	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18	°C/W

Power Ratings

Table 9. Pai8451 Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D Maximum power dissipation on both sides	$V_{CC1} = 5V$, $V_{CC2} = 5V$, $T_J = 150^\circ C$, $R_L = 60\Omega$, A repetitive pattern on TXD with 1 ms period, 990 μs LOW time, and 10 μs HIGH time.			438	mW
P_{D1} Maximum power dissipation on logic side				25	mW
P_{D2} Maximum power dissipation on bus side				413	mW

Safety Limiting Values

Table 10. Pai8451 Safety Limiting Values

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WB SOIC-16 Package					
I _S	Safety input, output, or supply current	R _{θJA} = 81°C/W, V _{CC1} = 5.5 V, V _{CC2} = 5.0 V, T _J = 150°C, T _A = 25°C		280	mA
		R _{θJA} = 81°C/W, V _{CC1} = 3.6 V, V _{CC2} = 5.0 V, T _J = 150°C, T _A = 25°C		429	mA
		R _{θJA} = 81°C/W, V _{CC1} = 2.75 V, V _{CC2} = 5.0 V, T _J = 150°C, T _A = 25°C		561	mA
P _S	Safety input, output, or total power, see Figure 4	R _{θJA} = 81°C/W, T _J = 150°C, T _A = 25°C		1543	mW
T _S	Maximum safety temperature			150	°C

Electrical Specifications: Supply current

Table 11. Pai8451 supply current specifications

V_{CC1} = 2.5V_{DC} ~ 5V_{DC}, 0.1μF capacitor from V_{CC1} to GND₁, V_{CC2} = 5V_{DC}, 1μF capacitor from V_{CC2} to GND₂. T_A = -40°C to 125°C (Unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I _{CC1} V _{CC2} = 5V	V _{TXD} = 0V		1.5	1.9	mA
	V _{TXD} = V _{CC1}		0.8	1.1	mA
I _{CC2}	V _{TXD} = 0V, R _L = 60Ω		50	75	mA
	V _{TXD} = V _{CC1}		6	14	mA

Electrical Specifications: Driver

Table 12. Pai8451 Electrical Specifications

V_{CC1} = 2.5V_{DC} ~ 5V_{DC}, 0.1μF capacitor from V_{CC1} to GND₁, V_{CC2} = 5V_{DC}, 1μF capacitor from V_{CC2} to GND₂. T_A = -40°C to 125°C (Unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{O(D)CANH}	Bus output voltage (Dominant) CANH V _I = 0 V, R _L = 60 Ω, see Figure 10	2.75	3.5	4.5	V
V _{O(D)CANL}	Bus output voltage (Dominant) CANL V _I = 0 V, R _L = 60 Ω, see Figure 10	0.5	1.5	2.25	V
V _{O(R)}	Bus output voltage (Recessive) V _I = V _{CC1} , R _L = 60 Ω, see Figure 11	2	0.5*V _{CC2}	3	V
V _{OD(D)}	Differential output voltage (Dominant) V _I = 0 V, R _L = 60 Ω, see Figure 11	1.5		3	V
V _{OD(R)}	Differential output voltage (Recessive) V _I = V _{CC1} , R _L = 60 Ω, see Figure 11	-0.1		0.1	V
	V _I = V _{CC1} , No Load, see Figure 11	-0.2		0.2	V
V _{OC(D)}	Common-mode output voltage (Dominant) see Figure 10	2	0.5*V _{CC2}	3	V
I _{IL}	TXD pin low-level input current V _I at 0.8 V, absolute value		1	10	μA
I _{OS(SS)}	Short-circuit steady-state output current, TXD=0V -15 V < V _{CANH} < 40 V, CANL Open	-100		100	mA
	-15 V < V _{CANL} < 40 V, CANH Open	-100		100	mA
C _O	Output capacitance See receiver input capacitance			20	pF
CMTI	Common-mode transient immunity V _{TXD} = V _{CC1} or 0 V, see Figure 19	50	80		kV/μs
V _{sym-dom}	Output symmetry (dominant) (V _{O(CANH)} + V _{O(CANL)}) / V _{CC2} R _L = 60 Ω, TXD = 0V	90		110	%
V _{sym-res}	Output symmetry (recessive) (V _{O(CANH)} + V _{O(CANL)}) / V _{CC2} R _L = 60 Ω, TXD = V _{CC}	90		110	%
V _{IT+(TXD)}	Positive-going TXD input threshold voltage		50	60	% of V _{CC1}
V _{IT-(TXD)}	Negative-going TXD input threshold voltage	30	35		% of V _{CC1}
V _{HYS(TXD)}	Hysteresis voltage (V _{IT+(TXD)} - V _{IT-(TXD)})		15		% of V _{CC1}

Electrical Specifications: Receiver

Table 13. Pai8451 Electrical Specifications

$V_{CC1} = 2.5V_{DC} \sim 5V_{DC}$, 0.1uF capacitor from V_{CC1} to GND₁, $V_{CC2} = 5V_{DC}$, 1uF capacitor from V_{CC2} to GND₂. $T_A = -40^{\circ}C$ to $125^{\circ}C$ (Unless otherwise noted).

PARAMETER	Comments	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT+(Bus)}$	Positive-going bus differential input threshold voltage				900	mV
$V_{IT-(Bus)}$	Negative-going bus differential input threshold voltage		500			mV
$V_{HYS(Bus)}$	Hysteresis voltage ($V_{IT+(Bus)} - V_{IT-(Bus)}$)			120		mV
V_{OH}	RXD High-level output voltage	$I_{OH} = -2\text{ mA}$	$V_{CC1} - 0.2$	$V_{CC1} - 0.1$		V
V_{OL}	Low-level output voltage	$I_{OL} = 2\text{ mA}$		0.1	0.2	V
C_i	Input capacitance to ground ⁽¹⁾ , (CANH or CANL)	TXD at V_{CC1} , $V_i = 0.4 \sin(4E6\pi t) + 2.5\text{ V}$ Guaranteed by design			24	pF
C_{ID}	Differential input capacitance ⁽¹⁾ , (CANH or CANL)	TXD at V_{CC1} , $V_i = 0.4 \sin(4E6\pi t)$ Guaranteed by design			12	pF
R_{ID}	Differential input resistance ⁽¹⁾	TXD at V_{CC1} Guaranteed by design	19	30	52	k Ω
R_{IN}	Input resistance (CANH or CANL) ⁽¹⁾	TXD at V_{CC1} Guaranteed by design	9	15	28	k Ω
$R_{I(m)}$	Input resistance matching ⁽¹⁾ $(1 - [R_{IN(CANH)} / R_{IN(CANL)}]) \times 100\%$	$V_{CANH} = V_{CANL}$ Guaranteed by design	-2		2	% ⁽²⁾
CMTI	Common-mode transient immunity ⁽¹⁾	$V_{TXD} = V_{CC1}$ or 0 V	50	80		kV/ μ s

(1) Not tested in production, guaranteed by design.

(2) This spec limit is only for $T_A = 25^{\circ}C$

Electrical Specifications: Device

Table 14. Pai8451 Electrical Specifications

$V_{CC1} = 2.5V_{DC} \sim 5V_{DC}$, 0.1uF capacitor from V_{CC1} to GND₁, $V_{CC2} = 5V_{DC}$, 1uF capacitor from V_{CC2} to GND₂. $T_A = -40^{\circ}C$ to $125^{\circ}C$ (Unless otherwise noted).

PARAMETER	Comments	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{loop1}	Total loop delay, driver input TXD to receiver output RXD, Recessive to Dominant	See Figure 20, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, $C_{L(RXD)} = 15\text{ pF}$; input rise/fall time (between 10% and 90%) on TXD = 2.9 ns; see Figure 17	70	120	220	ns
t_{loop2}	Total loop delay, driver input to receiver output, Dominant to Recessive	See Figure 20, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, $C_{L(RXD)} = 15\text{ pF}$; input rise/fall time (between 10% and 90%) on TXD = 2.9 ns; see Figure 17	70	130	220	ns
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)} = 500\text{ ns}$	See Figure 21, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, $C_{L(RXD)} = 15\text{ pF}$; input rise/fall time (between 10% and 90%) on TXD = 2.9 ns; see Figure 18	435		530	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)} = 200\text{ ns}$	See Figure 21, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, $C_{L(RXD)} = 15\text{ pF}$; input rise/fall time (between 10% and 90%) on TXD = 2.9 ns; see Figure 18	155		210	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)} = 500\text{ ns}$	See Figure 21, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, $C_{L(RXD)} = 15\text{ pF}$; input rise/fall time (between 10% and 90%) on TXD = 2.9 ns; see Figure 18	400		550	ns
	Bit time on RXD output pins with $t_{BIT(TXD)} = 200\text{ ns}$	See Figure 21, $R_L = 60\ \Omega$, $C_L = 100\text{ pF}$, $C_{L(RXD)} = 15\text{ pF}$; input rise/fall time (between 10% and 90%) on TXD = 2.9 ns; see Figure 18	120		220	ns
Δt_{REC}	Receiver timing symmetry with $t_{BIT(TXD)} = 500\text{ ns}$		-65		+40	ns
	Receiver timing symmetry with $t_{BIT(TXD)} = 200\text{ ns}$		-45		+15	ns

Electrical Specifications: Driver

Table 15. Pai8451 Electrical Specifications

$V_{CC1} = 2.5V_{DC} \sim 5V_{DC}$, 0.1 μ F capacitor from V_{CC1} to GND₁, $V_{CC2} = 5V_{DC}$, 1 μ F capacitor from V_{CC2} to GND₂. $T_A = -40^{\circ}\text{C}$ to 125°C (Unless otherwise noted).

PARAMETER	Comments	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pHR}	Propagation delay time, HIGH TXD to driver recessive	$R_L = 60\ \Omega$ and $C_L = 100\ \text{pF}$; input rise/fall time (10% to 90%) on TXD = 2.9 ns; see Figure 12 and Figure 13		100		ns
t_{pLD}	Propagation delay time, LOW TXD to driver dominant			75		ns
t_R	Differential output signal rise time ⁽¹⁾	$R_L = 60\ \Omega$ and $C_L = \text{open}$; see Figure 12 and Figure 13		45		ns
t_F	Differential output signal fall time ⁽¹⁾	$R_L = 60\ \Omega$ and $C_L = \text{open}$; see Figure 12 and Figure 13		45		ns
t_{TXD_DTO}	Dominant time out on TXD	$R_L = 60\ \Omega$ and $C_L = \text{open}$; see Figure 16	0.8	3	6.5	ms

(1) Not tested in production, guaranteed by design.

Electrical Specifications: Receiver

Table 16. Pai8451 Electrical Specifications

$V_{CC1} = 2.5V_{DC} \sim 5V_{DC}$, 0.1 μ F capacitor from V_{CC1} to GND₁, $V_{CC2} = 5V_{DC}$, 1 μ F capacitor from V_{CC2} to GND₂. $T_A = -40^{\circ}\text{C}$ to 125°C (Unless otherwise noted).

PARAMETER	Comments	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{pRH}	Propagation delay time, bus recessive input to RXD high output	$C_{L(RXD)} = 15\text{pF}$, see Figure 14 and Figure 15		120		ns
T_{pDL}	Propagation delay time, bus dominant input to RXD low output	$C_{L(RXD)} = 15\text{pF}$, see Figure 14 and Figure 15		80		ns
t_R	RXD output signal rise time ⁽¹⁾	$C_{L(RXD)} = 15\text{pF}$		2	10	ns
t_F	RXD output signal fall time ⁽¹⁾	$C_{L(RXD)} = 15\text{pF}$		2	10	ns

(1) Not tested in production, guaranteed by design.

INSULATION AND SAFETY RELATED SPECIFICATIONS**Insulation Specifications**

Table 17. Pai8451 Insulation Specifications

PARAMETER	SYMBOL	VALUE	UNIT	TEST CONDITIONS/COMMENTS
Rated Dielectric Insulation Voltage	V_{ISO}	5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	≥ 8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	≥ 8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		≥ 21	μm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	≥ 600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I		Material Group (DIN VDE 0110, 1/89, Table 1)

Package Specifications

Table 18. Pai8451 Package Specifications

PARAMETER	SYMBOL	VALUE	UNIT	TEST CONDITIONS/COMMENTS
Resistance (Input to Output) ¹	R _{I-O}	10 ¹²	Ω	V _{IO} =500V, T _A = 25°C
Resistance (Input to Output) ¹	R _{I-O}	10 ¹¹	Ω	V _{IO} =500V, T _A = 125°C
Resistance (Input to Output) ¹	R _{I-O}	10 ¹⁰	Ω	V _{IO} =500V, T _A = 150°C
Capacitance (Input to Output) ¹	C _{I-O}	1.5	pF	@300kHz

- (1) The device is considered a 2-terminal device; WB SOIC-16 Pin 1 - Pin 8 are shorted together as the one terminal, and WB SOIC-16 Pin 9 - Pin 16 are shorted together as the other terminal.

Regulatory Information

Table 19. Pai8451 Regulatory Information

The Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Regulatory	Pai8451-W1R
UL	Recognized under UL 1577 Component Recognition Program ¹ Single Protection, 5000 V _{RMS} Isolation Voltage File number: E494497
VDE	DIN EN IEC 60747-17 (VDE 0884-17): 2021-10 ² Basic insulation, V _{IORM} = 1200 V _{Peak} , V _{IOSM} = 5000 V _{Peak} ; File number: 40053041
CQC	Certified under CQC11-471543-2022 and GB4943.1-2022 Altitude ≤ 5000 m, Tropical Climate, Basic insulation at 1118 V _{RMS} (1580 V _{Peak}) maximum working voltage, Reinforced insulation at 557 V _{RMS} (788 V _{Peak}) maximum working voltage. File number: CQC23001387456
CB	Reinforced insulation per: IEC62368-1:2018. Max working voltage: 557 V _{RMS} , 788 V _{Peak} for WB SOIC-16 package. File number: CN59881

- (1) In accordance with UL 1577, each Pai8451 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.
(2) In accordance with DIN V VDE V 0884-11, each Pai8451 is proof tested by applying an insulation test voltage ≥ 1800V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-11 approval.

VDE Insulation Characteristics

Table 20. VDE Insulation Characteristics

DESCRIPTION	TEST CONDITIONS/COMMENTS	SYMBOL	CHARACTERISTIC	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive peak isolation voltage		V _{IORM}	1200	V _{Peak}
Input to Output Test Voltage, Method B1	V _{IORM} × 1.5 = V _{pd (m)} , 100% production test, t _{ini} = t _m = 1 sec, partial discharge < 5 pC	V _{pd (m)}	1800	V _{Peak}
Input to Output Test Voltage, Method A		V _{pd (m)}		
After Environmental Tests Subgroup 1	V _{IORM} × 1.3 = V _{pd (m)} , t _{ini} = 60 sec, t _m = 10 sec, partial discharge < 5 pC		1560	V _{Peak}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V _{IORM} × 1.2 = V _{pd (m)} , t _{ini} = 60 sec, t _m = 10 sec, partial discharge < 5 pC		1440	V _{Peak}
Highest Allowable Overvoltage		V _{IOTM}	7071	V _{Peak}
Surge Isolation Voltage Basic	Basic insulation, 1.2/50 μs combination wave, V _{TEST} = 1.3 × V _{IOSM} (qualification) ¹	V _{IOSM}	5000	V _{Peak}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure5)			
Maximum safety Temperature		T _S	150	°C
Maximum Power Dissipation at 25°C		P _S	1.14	W

DESCRIPTION	TEST CONDITIONS/COMMENTS	SYMBOL	CHARACTERISTIC	Unit
Insulation Resistance	$V_{IO} = 500\text{ V}$, $T_A = 25^\circ\text{C}$	R_{I-O}	$>10^{12}$	Ω
Insulation Resistance	$V_{IO} = 500\text{ V}$, $100^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$	R_{I-O}	$>10^{11}$	Ω
Insulation Resistance at T_S	$V_{IO} = 500\text{ V}$, $T_S = 150^\circ\text{C}$	R_{I-O}	$>10^9$	Ω

(1) In accordance with DIN V VDE V 0884-17, Pai8451 is proof tested by applying a surge isolation voltage 6500V.

TYPICAL CHARACTERISTIC

$V_{CC1} = 2.5V_{DC} \sim 5V_{DC}$, 0.1uF capacitor from V_{CC1} to GND₁, $V_{CC2} = 5V_{DC}$, 1uF capacitor from V_{CC2} to GND₂. $T_A = -40^\circ\text{C}$ to 125°C (Unless otherwise noted).

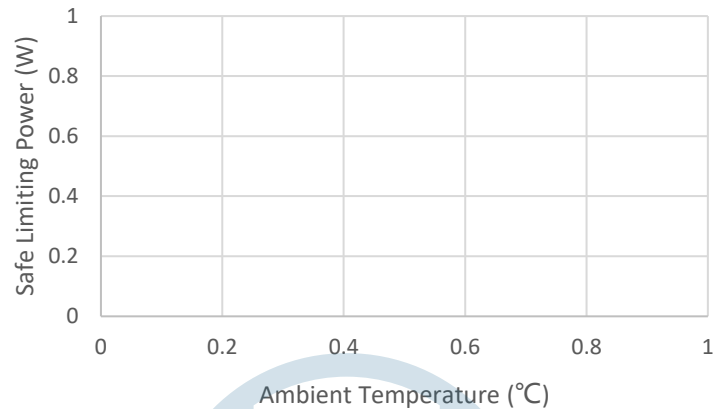


Figure 4. Thermal Derating Curve for Limiting Current per VDE

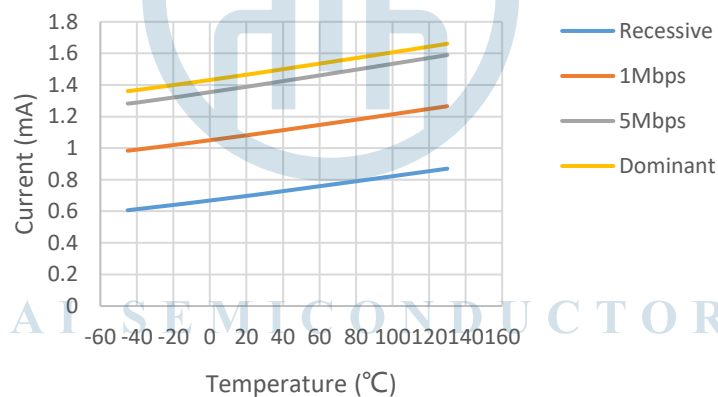


Figure 5. I_{CC1} vs Data Rate Over Ambient Temperature

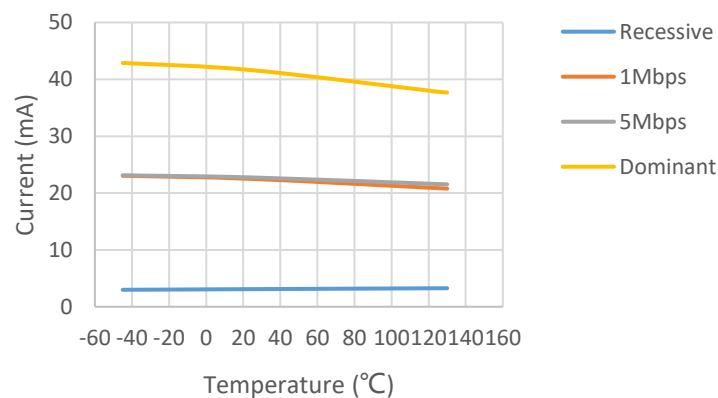


Figure 6. I_{CC2} vs Data Rate Over Ambient Temperature

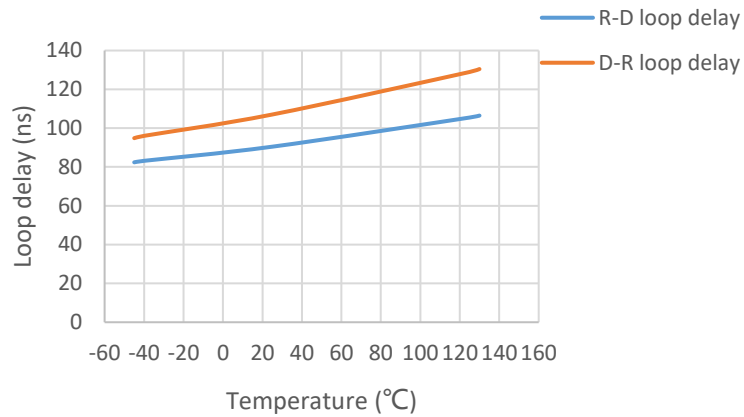
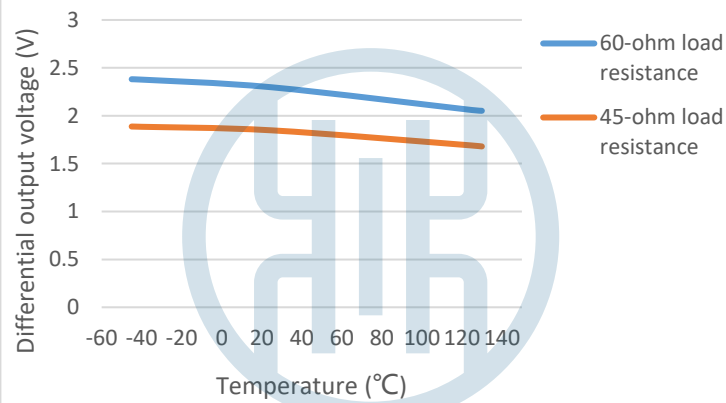
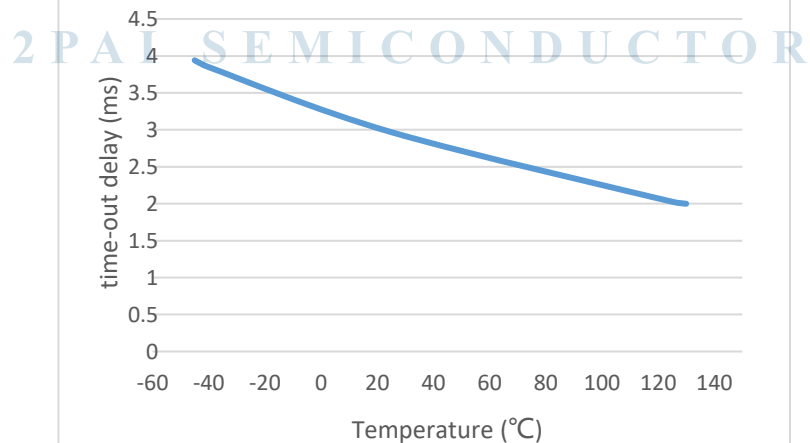


Figure 7. Loop Delay vs Ambient Temperature

Figure 8. $V_{OD(DOM)}$ vs Ambient TemperatureFigure 9. t_{TXD_DTO} vs Ambient Temperature

Parameter Measurement Information

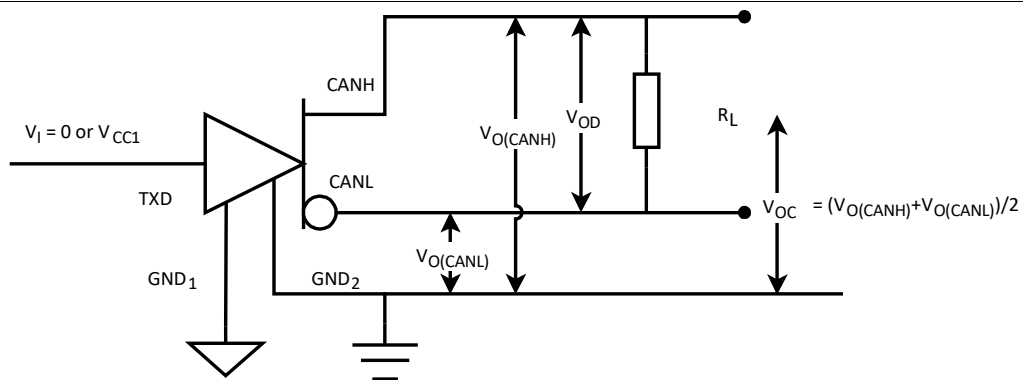


Figure 10. Driver Voltage Test Definitions

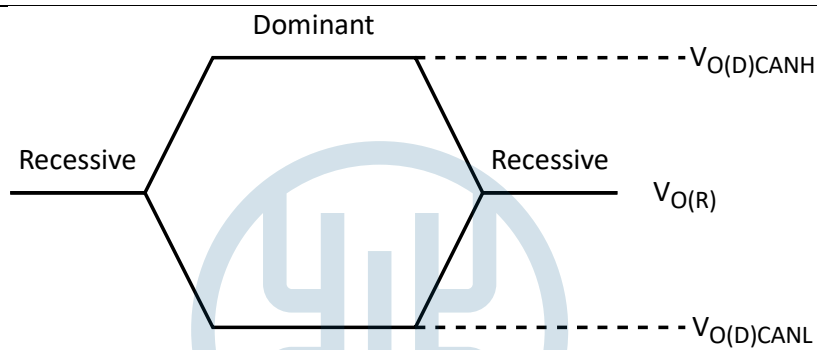
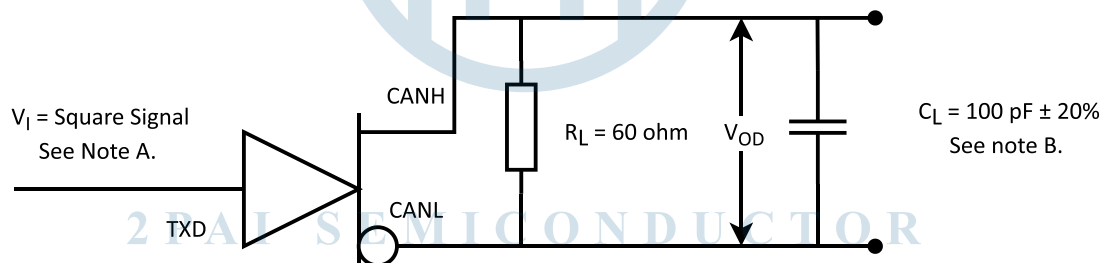


Figure 11. Bus Logic State Voltage Definitions



- A. The input square signal is supplied by a generator having the following spec: frequency = 500KHz, 50% duty cycle, $t_r < 10$ ns, $t_f < 10$ ns, $Z_0 = 50$ ohm.
 B. C. includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 12. Driver Propagation Delay Test Circuit

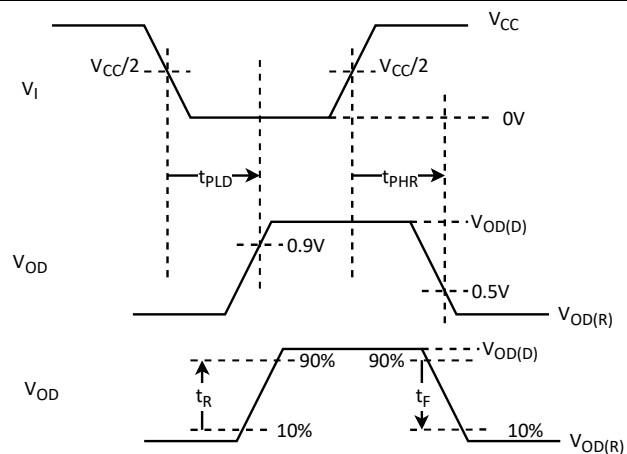
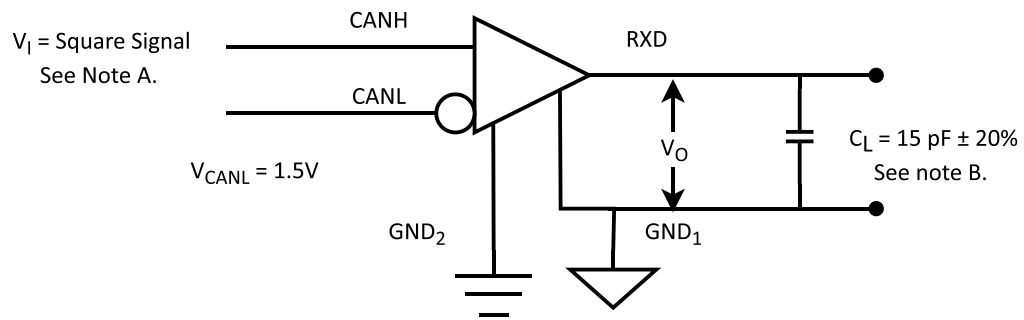


Figure 13. Driver Propagation Delay Waveforms



- A. The input square signal is supplied by a generator having the following spec: frequency = 500KHz, 50% duty cycle, $t_r < 10 \text{ ns}$, $t_f < 10 \text{ ns}$, $Z_o = 50 \text{ ohm}$.
- B. C_L includes instrumentation and fixture capacitance within $\pm 20\%$.

Figure 14. Receiver Test Circuit

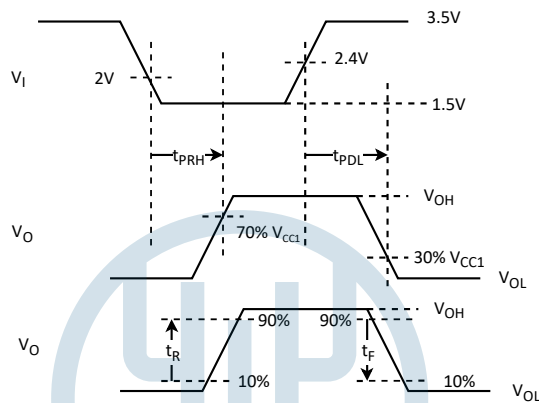


Figure 15. Receiver test waveforms

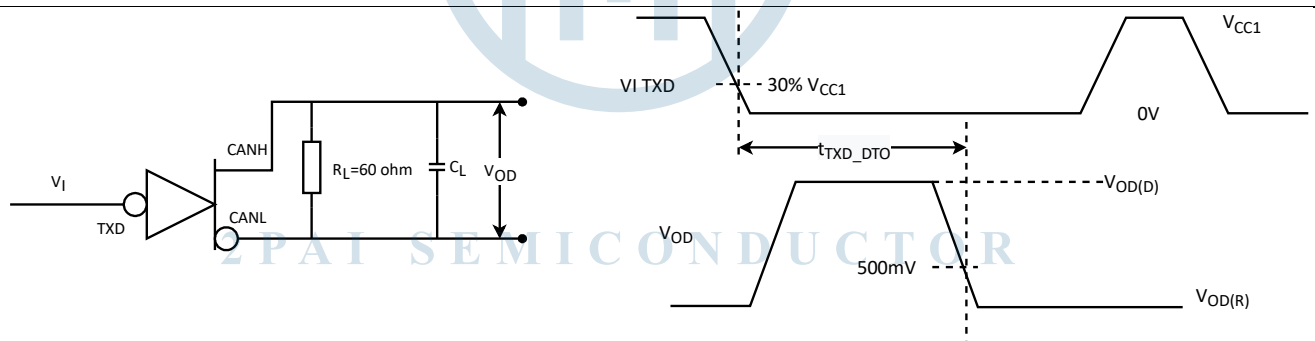


Figure 16. Dominant Time-out Test Circuit and Voltage Waveforms

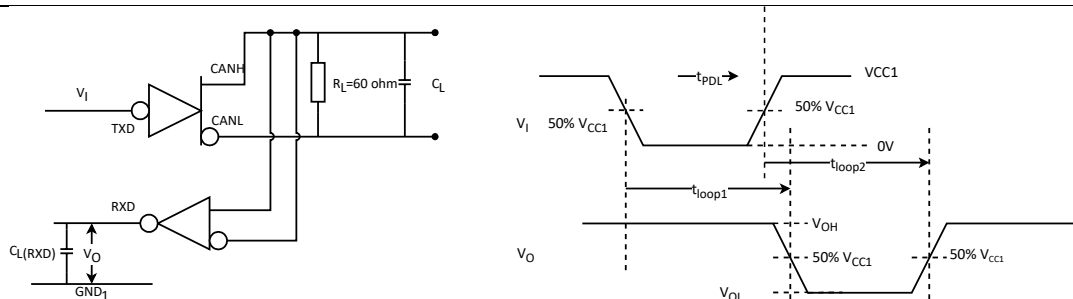


Figure 17. Device Loop Delay Test Circuit and Waveforms

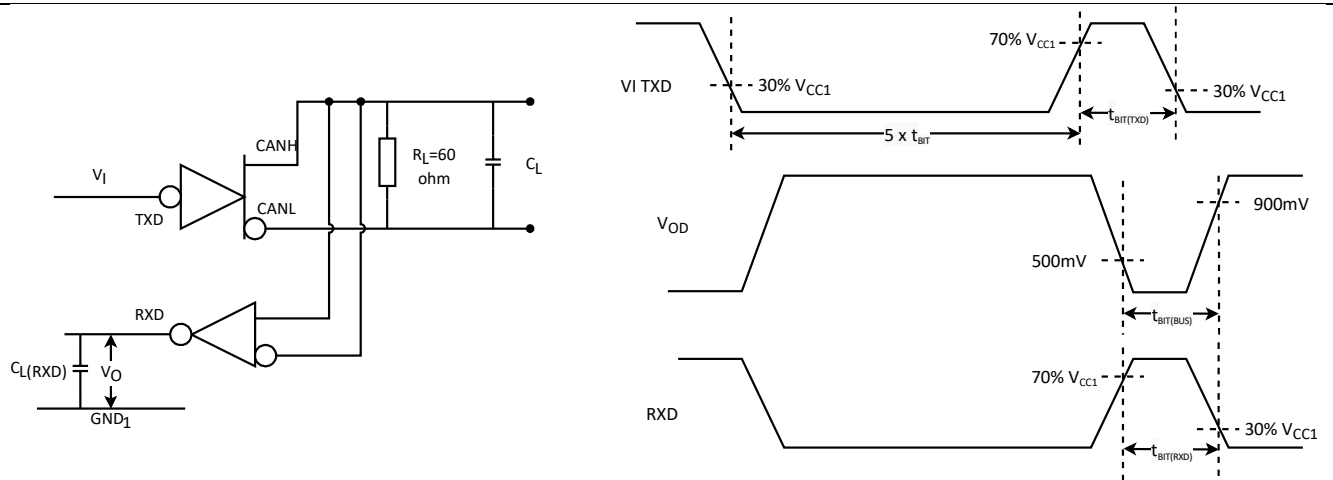


Figure 18. CAN FD Timing Parameter Test Circuit And Waveforms

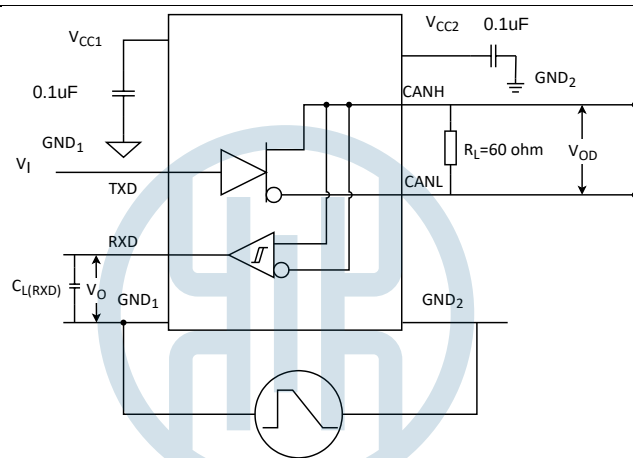


Figure 19. CMTI Test Circuit

OUTLINE DIMENSIONS

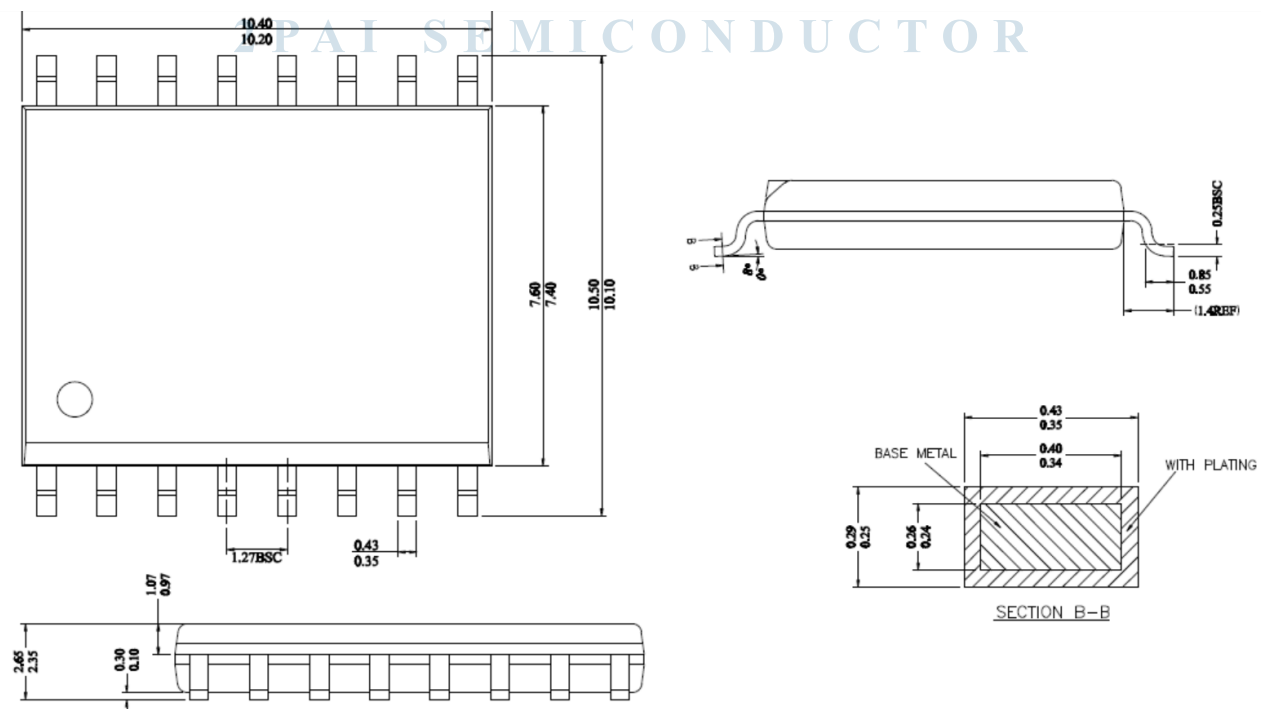


Figure 20. 16Lead Wide Body SOIC [WB SOIC-16] Outline Package—dimension unit(mm)

LAND PATTERNS

16-Lead Wide Body SOIC [WB SOIC-16]

The figure below illustrates the recommended land pattern details for the Pai8451 in a 16-pin wide-body SOIC. The table below lists the values for the dimensions shown in the illustration.

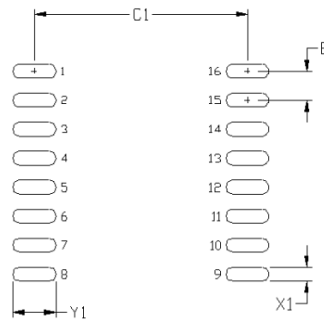


Figure 21. 16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern

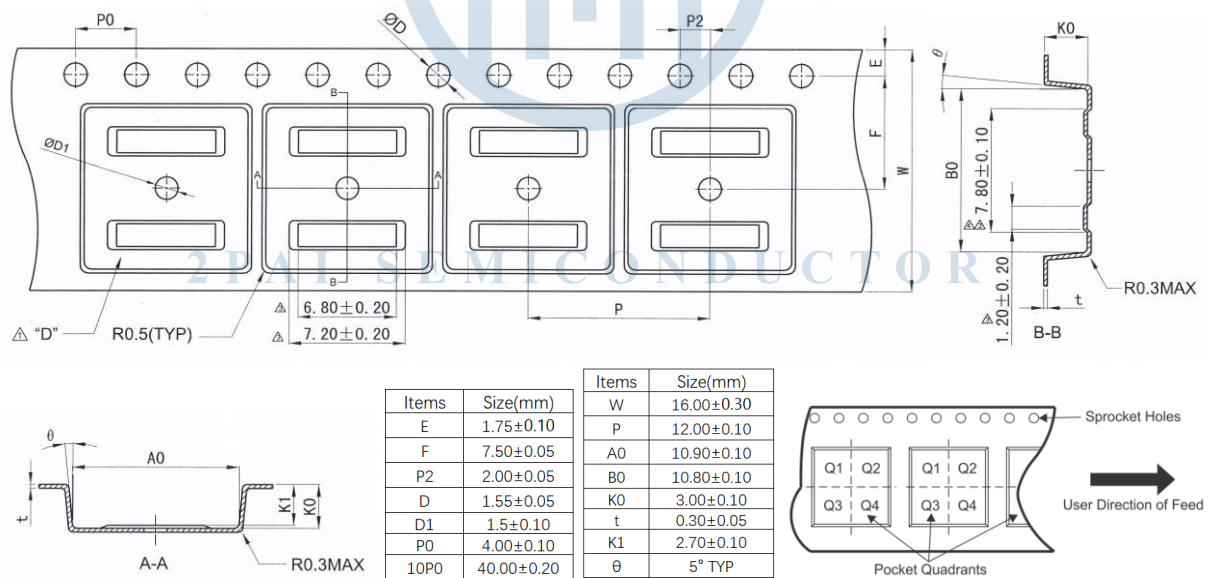
Table 21. WB SOIC-16 Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	9.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.90	mm

- (1) This land pattern design is based on IPC -7351.
- (2) All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

REEL INFORMATION

16-Lead Wide Body SOIC [WB SOIC-16]



Note: The Pin 1 of the chip is in the quadrant Q1

Figure 22. 16-Lead Wide Body SOIC [WB SOIC-16] Reel Information—dimension unit(mm)

Top Marking

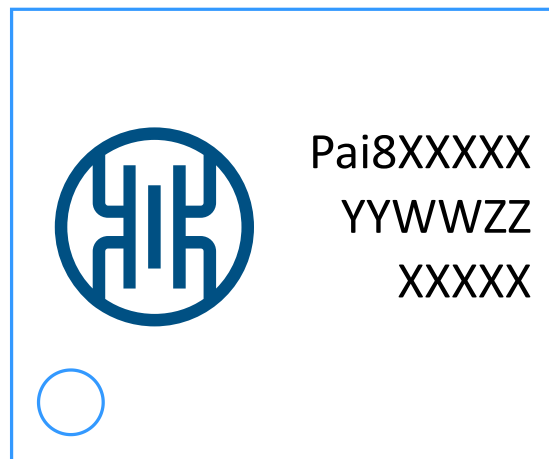


Figure 23. Top Marking

Line 1	Pai8XXXXX = Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXXX, no special meaning

ORDERING GUIDE

Table 22. Ordering Guide

Model Name	Temperature Range	Data Rate (Mbps)	Bus Protect Voltage (V)	Isolation Rating (kV rms)	Package	MSL Peak Temp ¹	MOQ/ Quantity per reel ²
Pai8451-W1R	-40 to 125°C	5	-40V ~ 40V	5.0	WB SOIC-16	Level-2-260C-1 YEAR	1500

- (1) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (2) MOQ, minimum ordering quantity.

2PAI SEMICONDUCTOR

REVISION HISTORY

Revision	Date	Page	Change Record
0.1	2022/10/12	All	Initial version
0.2	2024/7/4	6	In Table 13, the test condition of Item V_{OH} and V_{OL} is changed from 4mA to 2mA.
0.3	2024/10/24	14	Change the description in land pattern section
1.0	2025/4/17	15	Reliability qualification finished, change MSL description from 'Level2 verifying' to 'Level-2-260C-1 YEAR'

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