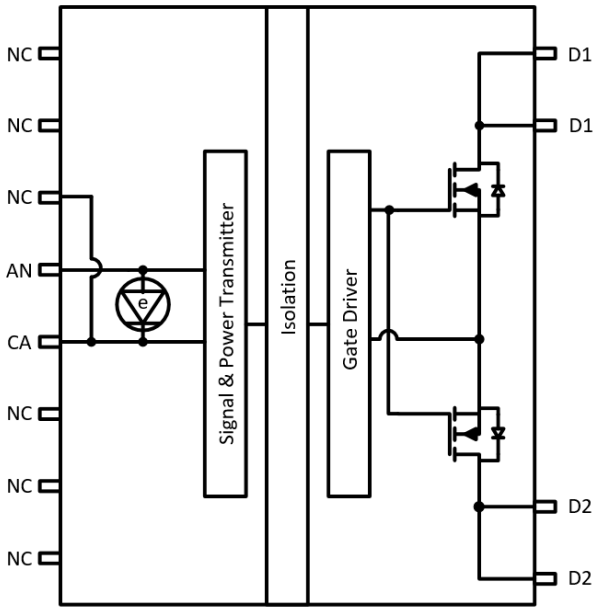
Features

- Compact bidirectional SiC MOSFETs
- Low output leakage current, $I_O \leq 1\mu A@V_{DS} = 1000V$
- Low on-resistance, $R_{ON}(Typ) = 100\Omega@I_O = 2mA$
- Low turn on time: $T_{ON} \leq 50\mu s$
- Low turn off time: $T_{OFF} \leq 200\mu s$
- 7V reverse breakdown voltage handling capability
- Stretched WB SOIC-12 package (derived from SOIC-16 with 4 pins removed) with ≥ 8 mm creepage&clearance
- Temperature range: -40°C to +125°C
- Safety-Related certifications:
  - VDE certificate number: 40056697

    Maximum peak repetitive voltage 1414V$_{PEAK}$ per DIN VDE V 0884-17:2021-10
  - UL certificate number: E494497

    5000V$_{RMS}$ for 1 min per UL1577
  - CQC certificate number: CQC23001378118
- AEC-Q100 qualified

Functional Block Diagram



Applications

- Battery/motor/solar panel insulation resistance measurement/leakage detection
- Sensing in high voltage application
- Electro-mechanical relay replacement
- Inrush current limiter protection

General Description

Pai8558EQ is an opto-compatible high-voltage isolated switch developed based on 2Pai Semi's unique isolation technology and mature standard semiconductor CMOS process. The device contains two SiC MOSFETs with bidirectional withstand voltage up to 1500V.

The input is isolated from the output by a 5kV$_{RMS}$ isolation barrier. It integrates a gate driver which controls the opening and closing of the two MOSFETs on the output. The output switches are turned on when the input current exceeds 7mA and turned off when the input voltage is lower than 0.4V.

The device uses a standard wide-body WB SOIC-12 package that provides 5kV$_{RMS}$ input-output withstand voltage, 10kV$_{PEAK}$ surge voltage and extremely high reliability.

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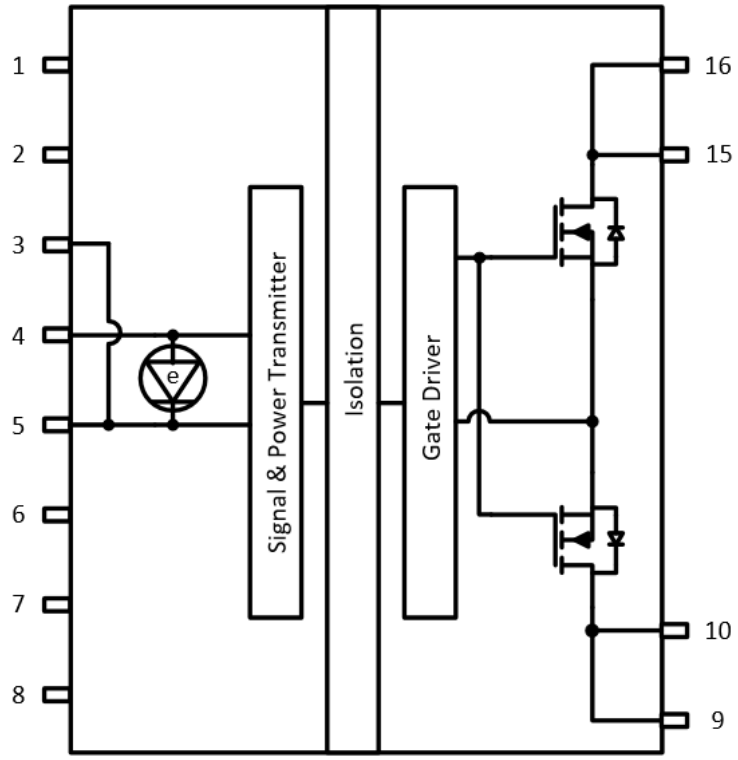
Contents

1 Pin Configurations and Functions

WB SOIC-12



Pin Functions

Pin No.	Pin Name	Type	Description
1,2,6,7,8	NC	-	No connection.
3	NC	-	Do not connect (internally connected to Pin 5).
4	AN	I	Anode.
5	CA	I	Cathode.
9,10	D2	O	Drain2.
15,16	D1	O	Drain1.

2 Specifications

2.1 Absolute Maximum Ratings (1)

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Unit
$I_{F(avg)}$	Average input current	T_A = -40°C to 125°C		30	mA
$I_{F(surge)}$	Surge input current	f = 1Hz, 50% duty		60	mA
I_{FP}	Peak transient input current	f = 100Hz, duty cycle = 0.1%		1	A
BVR	Reverse input voltage	T_A = -40°C to 125°C		7	V
P_{IN}	Input power dissipation			65	mW
I_O	Output load current	T_A = -40°C to 125°C		50	mA
I_{AV}	Output avalanche current	t_m = 1 min, duty cycle = 0.1%, cumulative of 5 mins over lifetime		0.6	mA
P_O	Output power dissipation			1000	mW
T_J	Junction temperature, T_J		-40	150	°C
T_A	Ambient temperature, T_A		-40	125	°C
T_{stg}	Storage temperature, T_{stg}		-55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2.2 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

Symbol	Parameter	Min	Max	Unit
$I_{F(ON)}$	Input current (ON)	7	20	mA
$V_{F(OFF)}$	Input voltage (OFF)	-5	0.4	V
V_O	Continuous load voltage		1000(1)	V
I_O	Load current	–10	10(2)	mA
T_A	Ambient temperature	-40	125	°C

(1) The maximum allowed withstand voltage refers to electrical characteristic tables.

(2) Recommended I_O can up to ±30mA within a safe junction temperature.

2.3 Insulation Specifications

Symbol	Parameter	Test Conditions	Value	Unit
CLR	External clearance	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage	Shortest pin-to-pin distance across the package surface	≥ 8	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
Material group		According to IEC 60664-1	I	

DIN EN IEC 60747-17 (VDE 0884-17):2021-10

Symbol	Description	Test Conditions	Value	Unit
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	1.2/50 µs waveform per IEC 62368-1 $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	6250	V_{PK}
$V_{pd(m)}$	Method a, after Input-Output safety test subgroup 2/3	$V_{ini} = V_{IOTM}$, t_{ini} = 60s $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s partial discharge ≤ 5 pC	1697	V_{PK}
	Method a, after Input-Output safety test subgroup 1	$V_{ini} = V_{IOTM}$, t_{ini} = 60s $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s partial discharge ≤ 5 pC	2263	V_{PK}
	Method b1, at routine test (100% production) and preconditioning (type test) (4)	Method b1: $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s partial discharge ≤ 5pC	2652	V_{PK}
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.4*sin(2πft), f =1MHz	~0.6	pF
R_{IO}	Isolation resistance, input to output (5)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500V at T_S =150°C	> 10^9	Ω
Pollution degree			2	
Climatic category			40/125/21	

2.4 ESD Rating

Parameter		Value	Unit
Electrostatic discharge	AEC-Q100-002-Rev E, HBM	±6000	V
	AEC-Q100-011-Rev D, CDM	±1000	

2.5 Electrical Characteristics

T_A = -40°C to 125°C, typical value is tested under T_A = 25°C, IF = 10mA, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_R	Input reverse breakdown voltage	I_R = 10uA	7			V
$V_{F(ON)}$	Input forward voltage	I_F = 10mA	1.9	2.0	2.2	V
$I_{F(ON)}$ (1)	Input current (ON)		1		7	mA
$\|V_{O(OFF)}\|$	Output withstand voltage	I_O = 100μA	1500			V
$I_{O(OFF)}$	Output leakage current	$V_{O=}$ 1000V			1000	nA
		V_O = 1500V			5000	nA
C_{OUT}	Output capacitance	V_O = 0V, f = 1MHz		2.5		pF
R_{ON}	Output resistance	I_O = 2mA		100	250	Ω

(1) The recommended $I_{F(ON)}$ should be higher than 7mA to ensure a complete ON in application.

2.6 Switching Characteristics

T_A = -40°C to 125°C, typical value is tested under T_A = 25°C, I_F=10mA, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{ON}	Turn-on time	I_F = 10mA, V_{DD} = 40V, R_{LOAD} = 20kΩ	5	15	50	μs
T_{OFF}	Turn-off time	V_{DD} = 40V, R_{LOAD} = 20kΩ	10	64	200	μs

2.7 Typical Characteristics

Typical value is tested under T_A = 25°C, I_F = 10mA, unless otherwise specified.

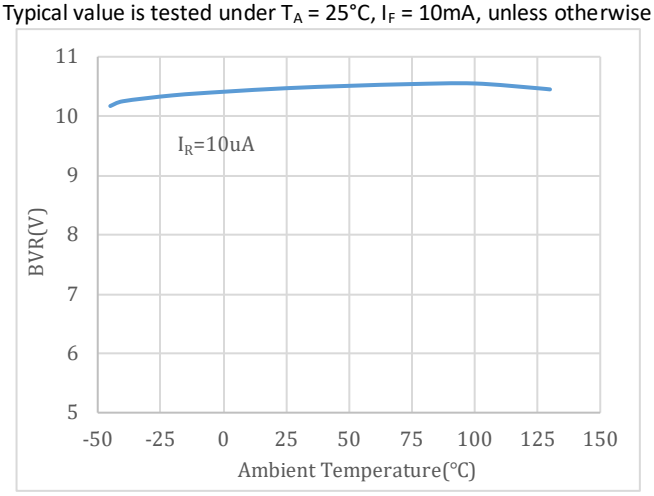


Figure 1. BVR vs Ambient temperature

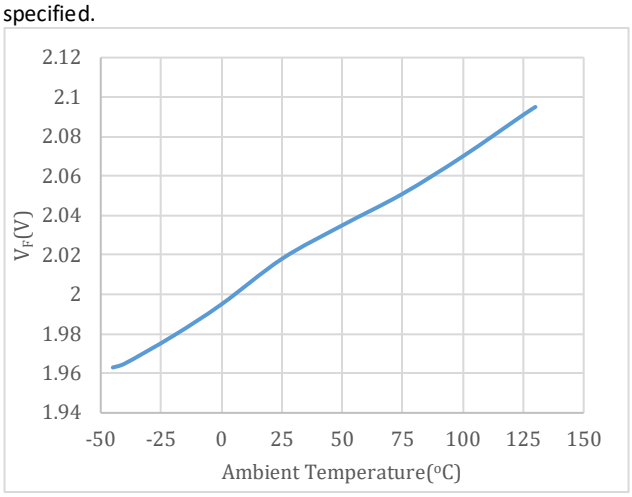


Figure 2. V_F vs Ambient temperature

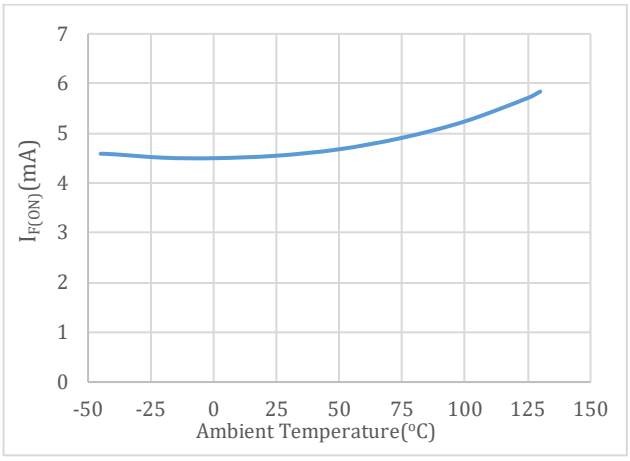


Figure 3. $I_{F(ON)}$ vs Ambient temperature

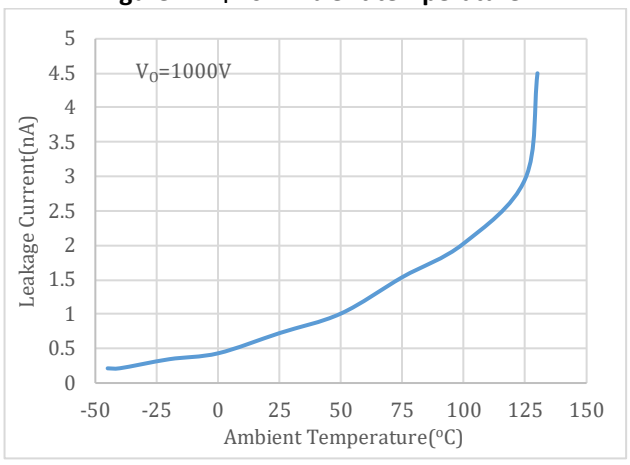


Figure 4. Leakage current vs T_A

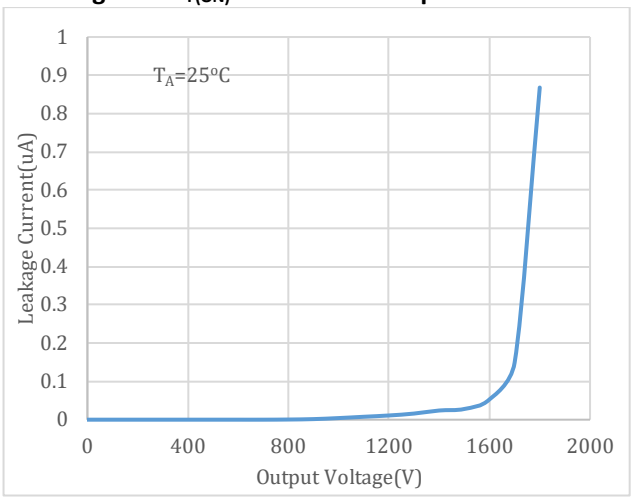


Figure 5. Leakage current vs Output voltage

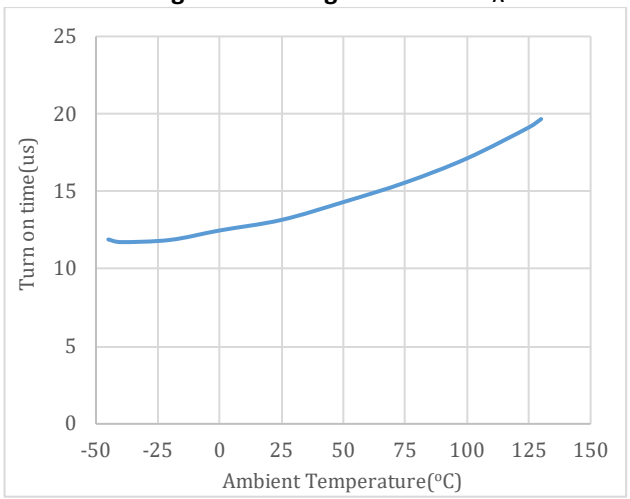


Figure 6. Turn-on time vs Ambient temperature

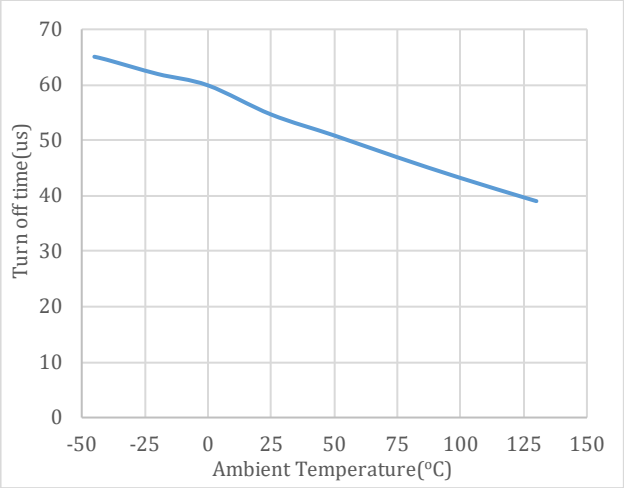


Figure 7. Turn-off time vs Ambient temperature

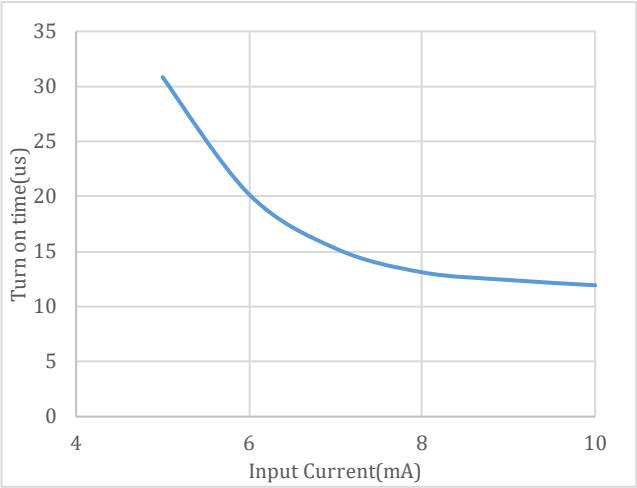


Figure 8. Turn-on time vs Input current

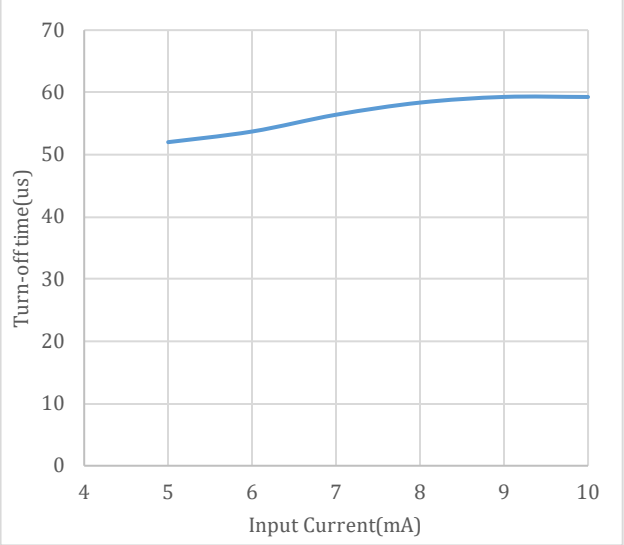


Figure 9. Turn-off time vs Input current

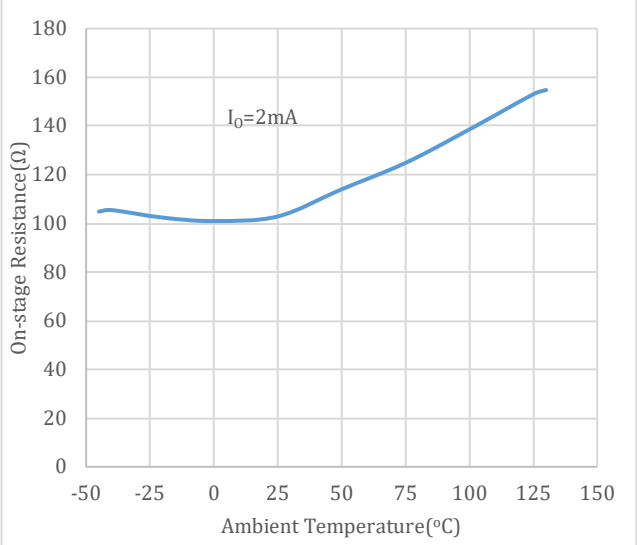


Figure 10. On-resistance vs Ambient temperature

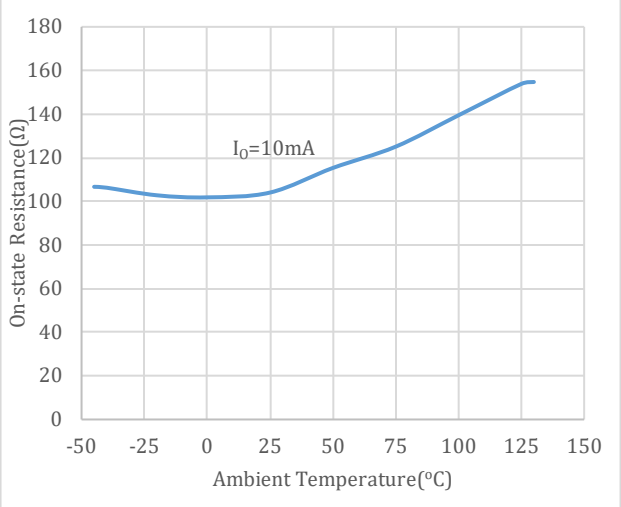


Figure 11. On-resistance vs Ambient temperature

3 Parameter Measurement Information

3.1 Switching Time Test Circuit and Waveform

Figure 12 shows how to measure turn-on & turn-off time.

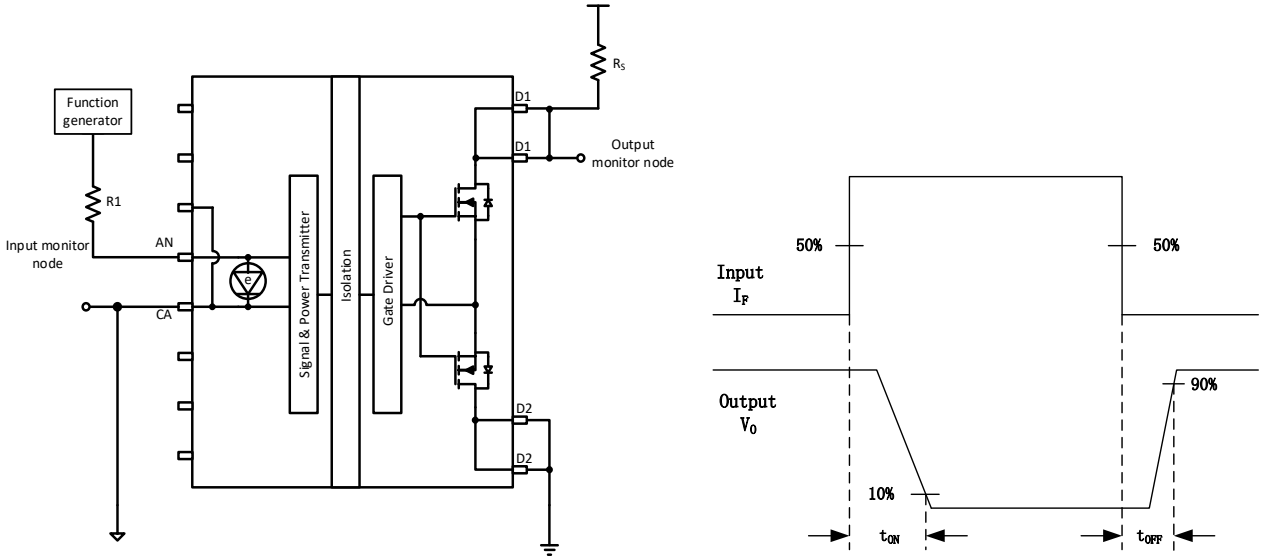


Figure 12. Switching time test circuit and waveform

4 Application Information

Pai8558EQ is a single channel isolated solid relay that is functionally equivalent an opto-coupler relay as shown in Figure 13. It functions like a bidirectional switch with no output power requirement. The recommended input current is 7mA to 20mA, which can totally make the output side in on-state.

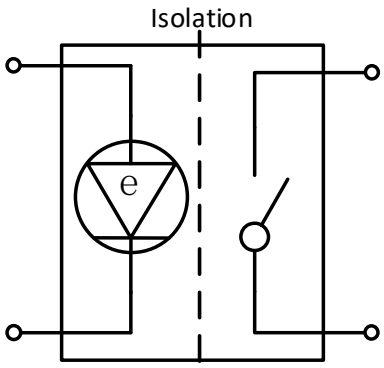


Figure 13. Pai8558EQ Equivalent Circuit

The input side energy is delivered through an on-chip power transfer block and implement a driver circuitry to switch two inner high-voltage SiC MOSFETS. When sufficient current is driven into current input side controller, the internal power delivery circuit will be enabled. Then the energy in the input side will be delivered to the output side to supply output side driving circuit to switch the inner two high voltage SiC MOSFETs. A typical application circuit (Figure 14) shows the Pai8558EQ's input being controlled by the microprocessor to switch the output (high voltage side).

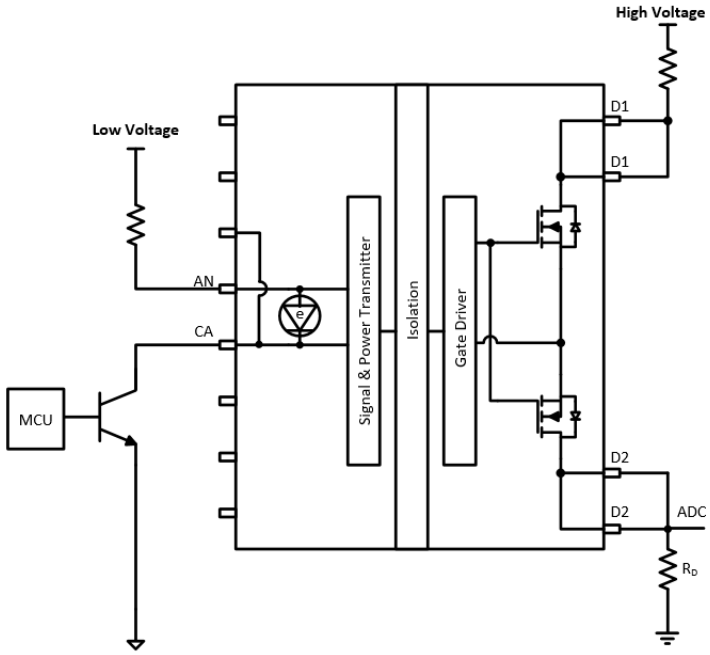


Figure 14. Typical Application Circuit

The Pai8558EQ 's galvanic isolation protects the low voltage side of the circuit (input) from the high-voltage side (output). Pins 9 and 10 are internally connected, and Pins 15 and 16 are internally connected too. It is recommended to shorting Pin 9 to Pin 10, as well as shorting Pin 15 to Pin 16 while arranging the PCB layout.

4.1 EMI Consideration

Different from traditional solid relay, Pai8558EQ is designed based on 2Pai semi's unique isolation technique, internal energy transmission is entirely depended on electrical signal. Electromagnetic interference should be carefully considered, which mainly come from the equivalent common mode source between the primary side and the secondary side.

Below shows two effective methods to reduce the common-mode electromagnetic interference:

Add Ferried Beads in Primary Side

As shown in Figure 15, it is recommended to add two symmetrical ferried beads in primary side. The ferried bead's resonant frequency should be similar with Pai8558EQ's internal operation frequency (typical 133MHz). Meanwhile, bead impedance at the resonant frequency should be as large as possible (at least 4kΩ).

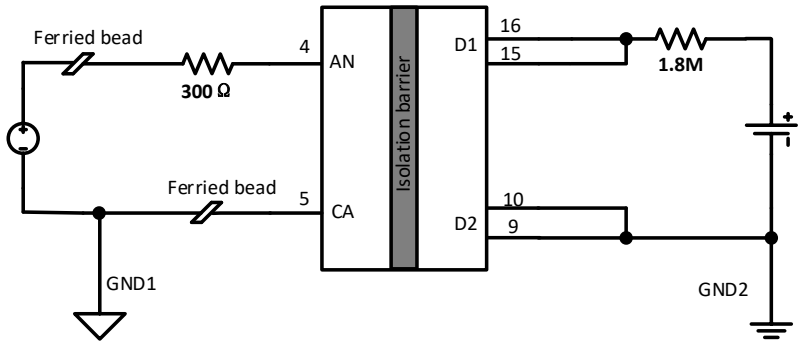


Figure 15. Typical Application Circuit

Split Resistors in Secondary Side

In typical applications, several large resistors in series are in high-voltage side close to D1. In this case, only the high side emissions can be dissipated. To damp the common-mode emissions, another effective method is dividing these resistors into two parts separately in D1 side and D2 side, as shown in Figure 16.

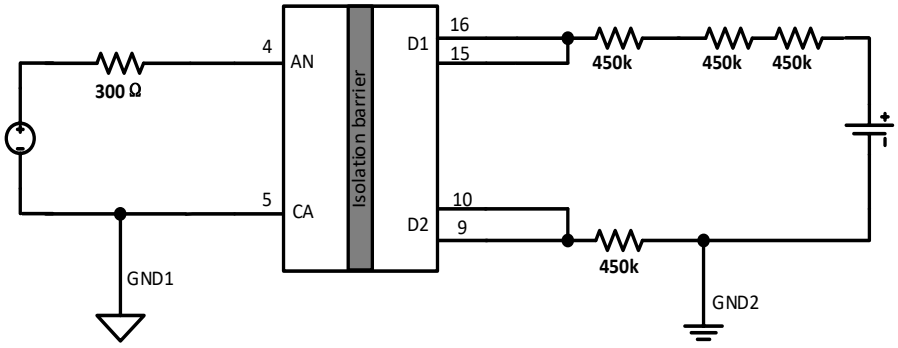


Figure 16. Typical Application Circuit

It should be noted that the total resistance should be constant, and the resistor's parasitic capacitance should be as small as possible.

4.2 Automotive Insulation Detection

Considering EMI and Bulk current injection (BCI) performance, Figure 17 shows the suggested insulation detection example diagram. Rx and Ry are insulation resistance, by turning on/off Pai8558EQ and monitoring the responding sampling points, Rx and Ry can be derived. D1 of U1 and D2 of U2 are interface ports, which are emitting noise and directly interfaced, hence, six high-value resistors (510k) are arranged in upper and lower sides. Meanwhile, to damp the in-board noise, the rest two 510k-resistors are in D2 of U1 and D1 of U2. Two 2*X caps in primary side are recommended to reserve to bypass inside/outside differential noise.

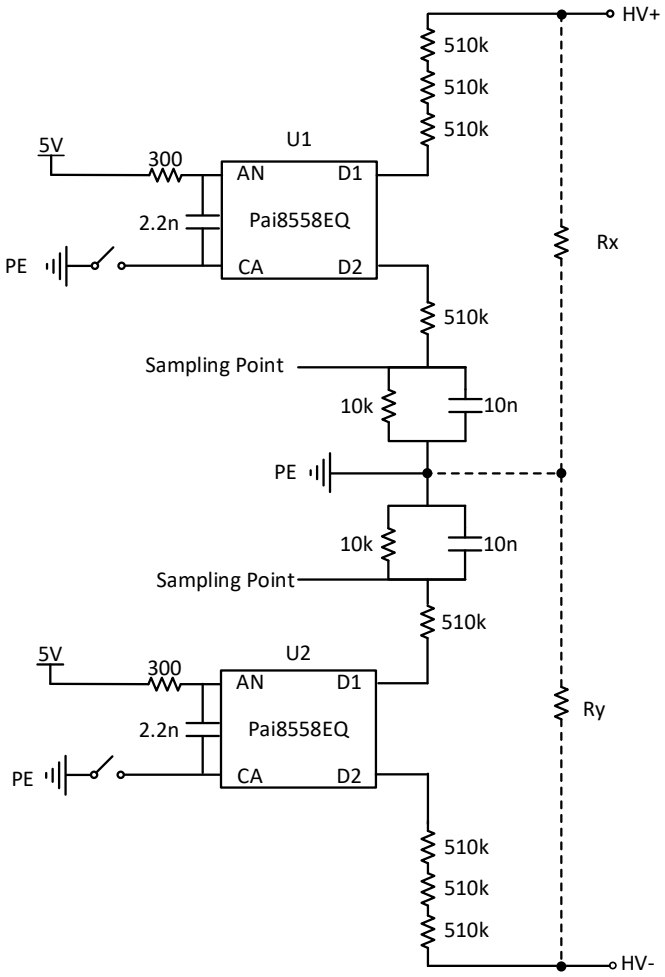
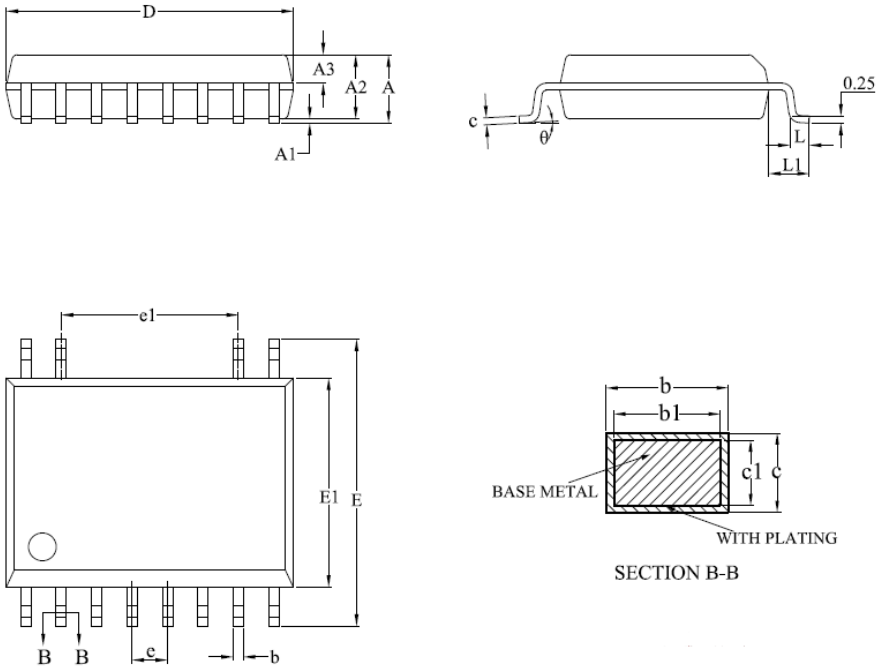


Figure 17. Example Insulation Detection Diagram

5 Outline Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	—	0.43
b1	0.34	0.37	0.40
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
e1	6.35BSC		
L	0.55	—	0.85
L1	1.40REF		
θ	0	—	8°

Figure 18. WB SOIC-12 Outline Package

6 Land Patterns

The Figure 18 illustrates the recommended land pattern details for the Pai8558EQ in a 12-pin wide body SOIC package.

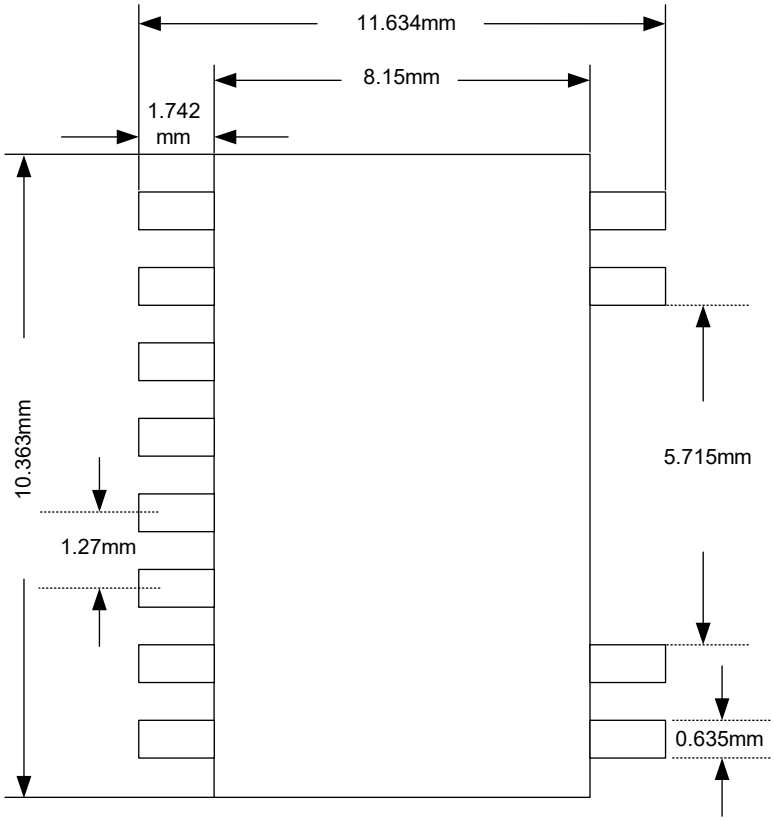


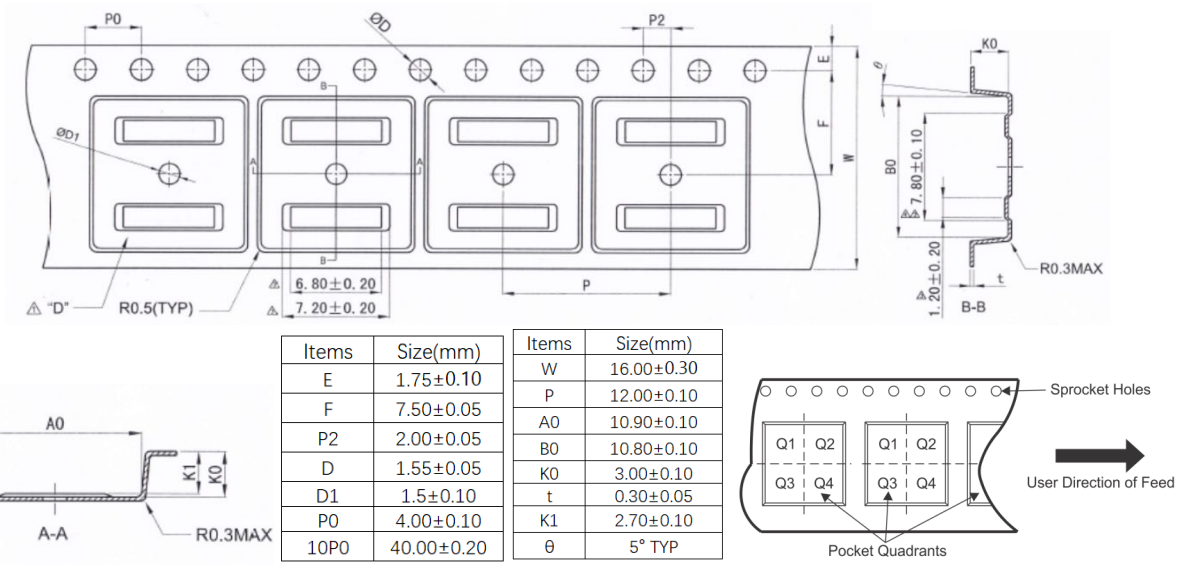
Figure 19. 12-Lead Wide Body SOIC [WB SOIC-12] Land Pattern

7 Top Marking

Figure 20. Top Marking

Line 1	PaiXXXXXX=Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXXX, no special meaning

8 Reel Information



Items	Size(mm)
E	1.75±0.10
F	7.50±0.05
P2	2.00±0.05
D	1.55±0.05
D1	1.5±0.10
P0	4.00±0.10
10P0	40.00±0.20

Items	Size(mm)
W	16.00±0.30
P	12.00±0.10
A0	10.90±0.10
B0	10.80±0.10
K0	3.00±0.10
t	0.30±0.05
K1	2.70±0.10
θ	5° TYP

Figure 21. WB SOIC-12 Reel Information–dimension unit(mm)

Note: The Pin 1 of the chip is in the quadrant Q1.

9 Ordering Guide

Model Name	Temperature Range	Withstand Voltage Rating(kV_{RMS})	Package	MSL Peak Temp	Quantity Per Reel
Pai8558EQ-W2R	-40~125°C	5.0	WB SOIC-12	Level-2-260°C-1Year	1500

Note: MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

10 Important Notice and Disclaimer

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11 Revision History

Revision	Date	Page	Change Record
Rev.0.1	2021-03-18	All	Initial version.
Rev.0.2	2022-11-04	Page 1, Page 5, Page 6, Page 7, Page 8, Page 10	Delete Truth Table in Page 1, add curves in Page 5, Page 6, add package dimension in Page 10, change figures in Page 1, 7, and 8, initial release
Rev.0.3	2023-04-20	Page 1, Page 4 Page 5, Page 7	Adjust the page layout in all pages, modify $V_{F(OFF)}$ spec in Page 5, add remarks for $I_{F(ON)}$&$V_{F(OFF)}$ in Page 5, add VDE certificate No in Page 1, add remarks for recommended I_O&V_O in Page 4, and add curve R_{ON} vs Ambient temperature in Page 7.
Rev.0.4	2023-09-26	Page 4, Page 5, Page 6, Page 8, Page 10	Delete symbol $V_{F(OFF)}$ in electrical characteristic table in Page 4, update curve data in Page 5&6, modify test circuit in Page 8, modify Figure 15 in Page 10.
Rev.1.0	2023-12-29	All	Release version.
Rev.1.1	2024-07-18	Page 5	Update safety-related certifications.
Rev.1.2	2024-12-03	Page 12	Update application information.