Features

- **Floating channel designed for bootstrap operation**
- **Fully operational to 700V**
- **Tolerant to negative transient voltage**
- **100 dv/dt immune**
- **Gate drive supply range from 10 to 20V**
- **Undervoltage lockout**
- **3.3V, 5V and 15V logic compatible**
- **Cross-conduction prevention logic**
- **Matched propagation delay for both channels**
- **Internal set deadtime**
- **High side output in phase with input**
- **Shut down input turns off both channels**

General Description

The Pai8171A is a 700 V high side and low side driver with 0.29 A source & 0.6 A sink current based on iDivider technology of 2Pai Semi. The Pai8171A are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 700 volts.

Device Information

Part Number	I_{PK}	Rec. VDD Supply Min.	Package
Pai8171A-SR	0.29A/0.6A	9.8V	NB SOIC-8

Functional Block Diagrams

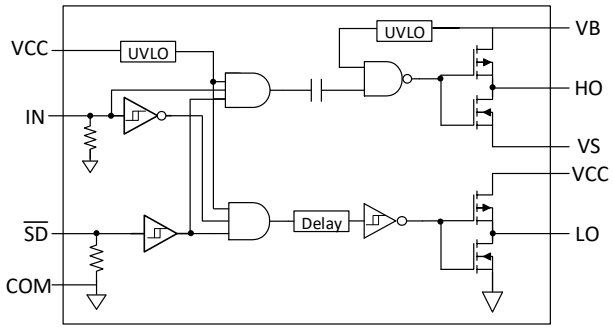

Fig 1. Pai8171A functional Block Diagram

Typical Connection Diagram

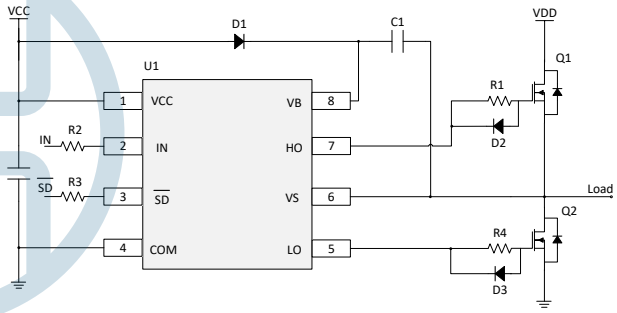

Fig 2. Pai8171A Typical Connection Diagram

Room 307-309, No.22, Boxia Road, Pudong New District, Shanghai, 201203, China
021-50850681

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1. Pin Configurations and Functions

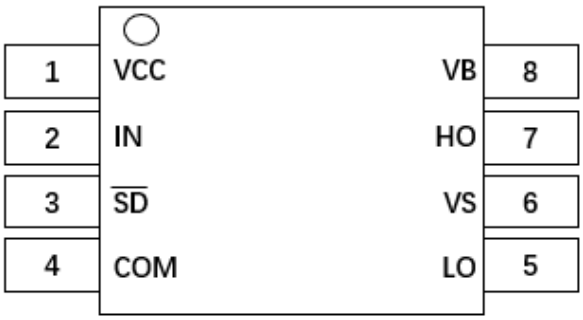


Fig 2. Pin Configuration

Pai8171A Pin Function Descriptions

PIN NO.	PIN NAME	DESCRIPTION
1	VCC	Low side and logic fixed supply
2	HIN	Logic input for high side and low side gate driver output (HO and LO), in phase with HO
3	$\overline{SD}$	Logic input for shutdown
4	COM	Low side return
5	LO	Low side gate drive output
6	VS	High side floating supply return
7	HO	High side gate drive output
8	VB	High side floating supply

2. Specifications

2.1.Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
Input voltage range	V_{CC}	−0.3 to 22	V
High side boot pin voltage to GND	V_B	−720 to 720	V
High side floating voltage	V_B–V_{VS}	−0.3 to 22	V
High side drive output voltage	V_{HO}	V_{HS} – 0.3 to V_B + 0.3	V
Low side drive output voltage	V_{LO}	−0.3 to V_{CC} + 0.3	V
Allowable VS slew rate	dV_{VS}/dt	100	V/ns
Drive input voltage	$V_{\overline{SD}}$,V_{HIN}	−0.3 to V_{CC} + 0.3	V
Junction temperature	$T_{J(MAX)}$	150	℃
Storage temperature range	T_{STG}	−55 to 150	℃
Lead Temperature Soldering Reflow (SMD Styles ONLY), Pb−Free Versions		260	℃

1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2.2.ESD Ratings

$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22- C101(2)	±1000	

2.3.Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VCC	VCC Input supply voltage	10	20	V
VB-VVS	Driver output bias supply	10	20	V
HIN-GND, $\overline{SD}$-GND	input voltage	GND	VCC	V
VLO	Low side output voltage	GND	VCC	V
VVS-GND	High Side Output Voltage	−700	700	V
VHO	High side output voltage	VS	VB	V
T_A	Ambient Temperature	–40	125	°C

2.4.Thermal Information

SYMBOL	PARAMETER	TYP	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	200	°C/W

3. Specifications

3.1.Electrical Characteristics

−40°C <T_J < 125°C, V_{CC} =V_B =15V, V_{VS} = GND, outputs are no loaded and all voltages are referenced to GND; unless otherwise noted, Typical values are at T_J = 25°C.

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CCQ}	VCC quiescent current	V_{HIN} = 0 V, V_{LIN} = 5 V		0.2		mA

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BQ}	VB quiescent current	V_{HIN} = 0 V, V_{LIN} = 5 V		0.45		mA
V_{VCC_ON}	VCC UVLO Rising threshold		8.4	9.1	9.8	V
V_{VCC_OFF}	VCC UVLO Falling threshold		7.6	8.3	9.0	V
V_{VCC_HYS}	UVLO Threshold hysteresis			0.8		V
V_{VB_ON}	UVLO Rising threshold		7.6	8.3	9.0	V
V_{VB_OFF}	UVLO Falling threshold		6.6	7.3	8.0	V
V_{VB_HYS}	UVLO Threshold hysteresis			1		V
V_{HIT}	Input high threshold voltage		2.0	2.2	2.4	V
V_{LIT}	Input low threshold voltage		1.1	1.3	1.5	V
V_{IHYS}	Input threshold hysteresis			0.9		V
I_{LO+}, I_{HO+}	Pai8171A Peak output source current	VLO=VHO=15V	0.13	0.29		A
I_{LO-}, I_{HO-}	Pai8171A Peak output sink current	VLO=VHO=0V	0.27	0.6		A
V_{OHA}, V_{OHB}	Output voltage at high state	IOUT = –2mA		14.95		V
V_{OLA}, V_{OLB}	Pai8171A Output voltage at low state	IOUT = 2 mA		20		mV
DT	Dead time	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off	400	520	650	ns
t_r	Rise time LO, HO	C_{load} = 1 nF		50	100	ns
t_f	Fall time LO, HO	C_{load} = 1 nF		30	60	ns
t_{on}	Turn-on Propagation delay	C_{load} = 1 nF		680	820	ns
t_{off}	Turn-off Propagation delay	C_{load} = 1 nF		130	220	ns
T_{MT}	Delay matching, HO & LO turn on/off	C_{load} = 1 nF			60	ns

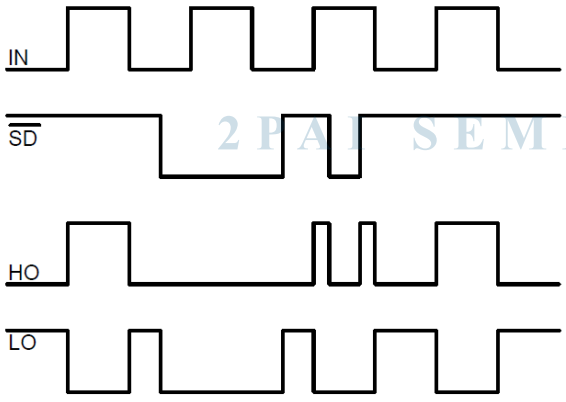


Fig 4. Input/Output Timing Diagram

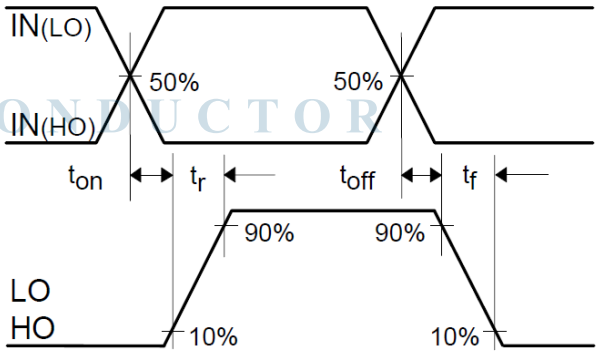


Fig 5. Switching Time Waveform Definitions

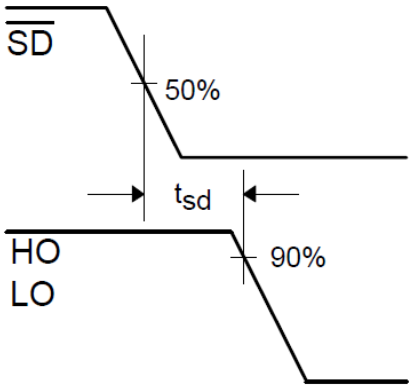


Fig 6. Shutdown Waveform Definitions

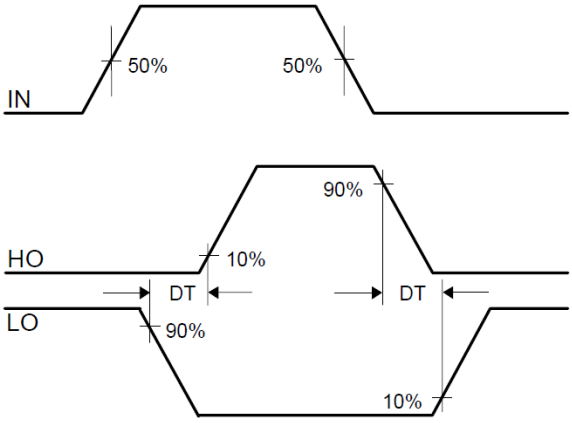


Fig 7. Deadtime Waveform Definitions

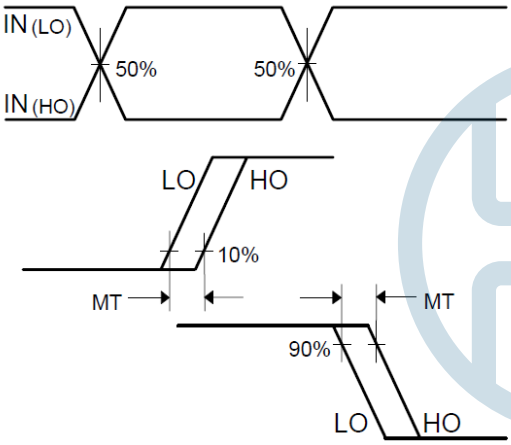


Fig 8. Delay Matching Waveform Definitions

3.2.Typical Characteristics

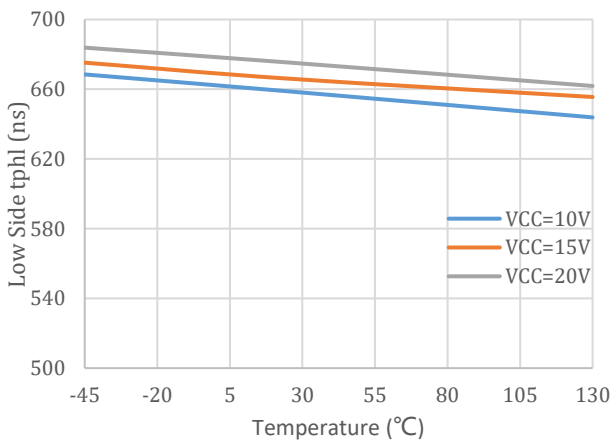


Fig 9. Low-Side, Turn-On Propagation Delay vs Temperature

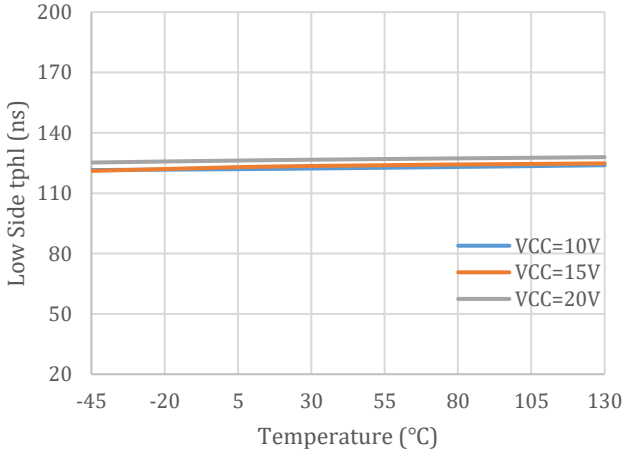


Fig10. Low-Side, Turn-Off Propagation Delay vs Temperature

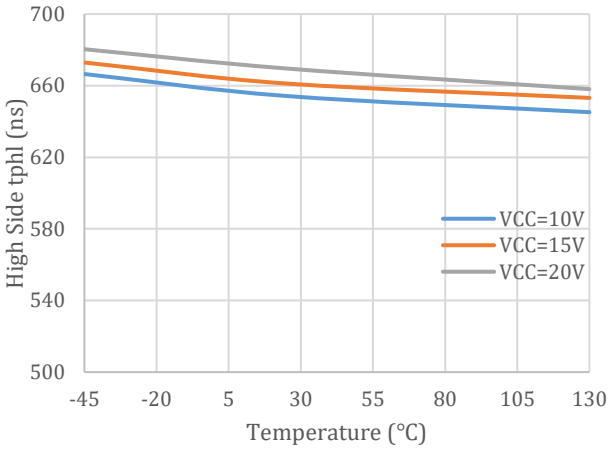


Fig 11. High-Side, Turn-On Propagation Delay vs Temperature

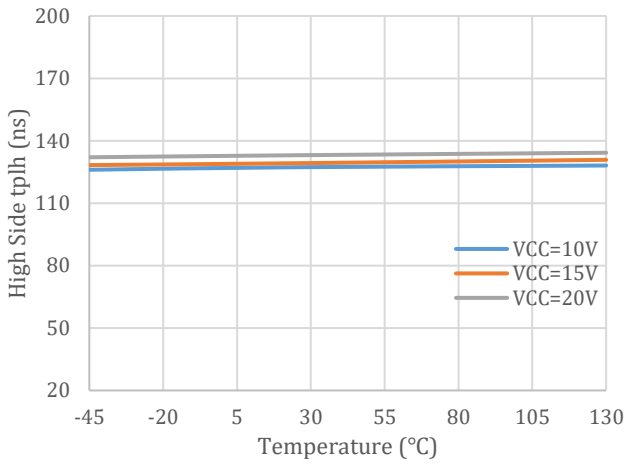


Fig 12. High-Side, Turn-Off Propagation Delay vs Temperature

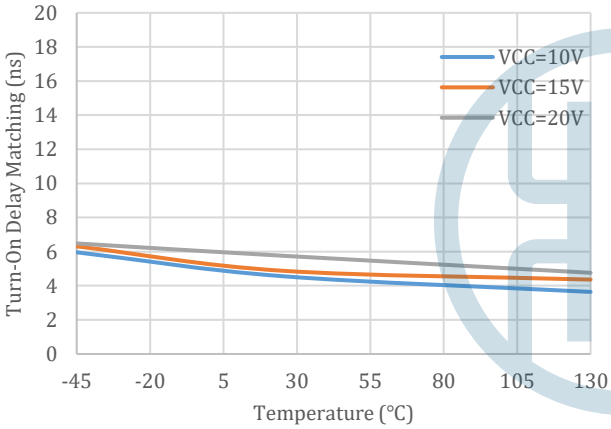


Fig 13. Turn-On Delay Matching vs Temperature

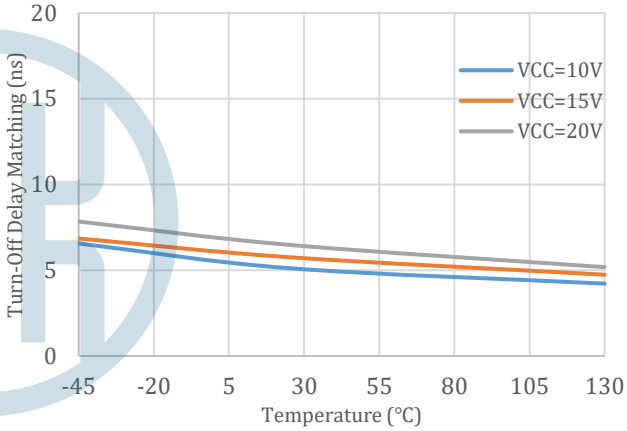


Fig 14. Turn-Off Delay Matching vs Temperature

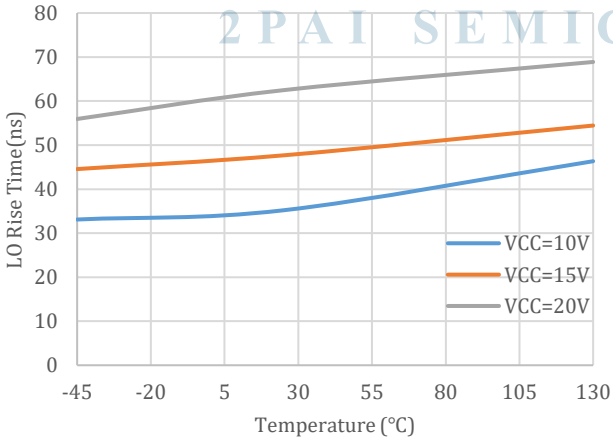


Fig 15. LO Rise Time with 1000-pF Load vs Temperature

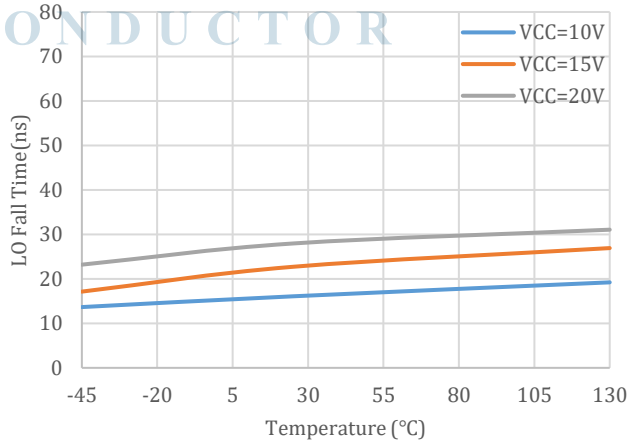


Fig 16. LO Fall Time with 1000-pF Load vs Temperature

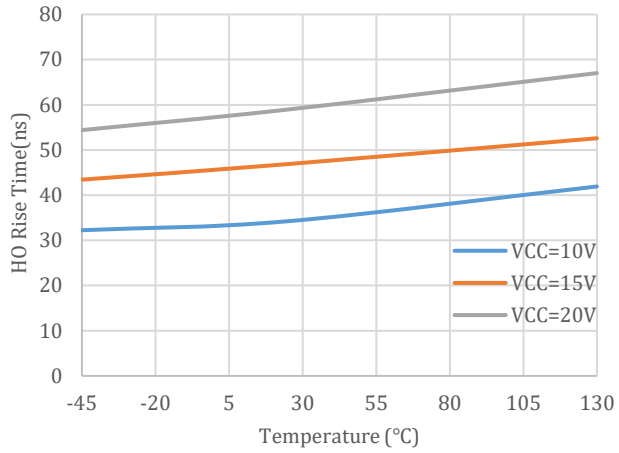


Fig 17. HO Rise Time with 1000-pF Load vs Temperature

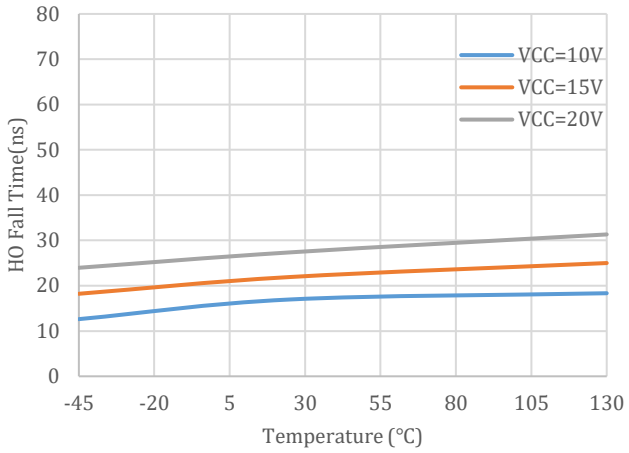


Fig 18. HO Fall Time with 1000-pF Load vs Temperature

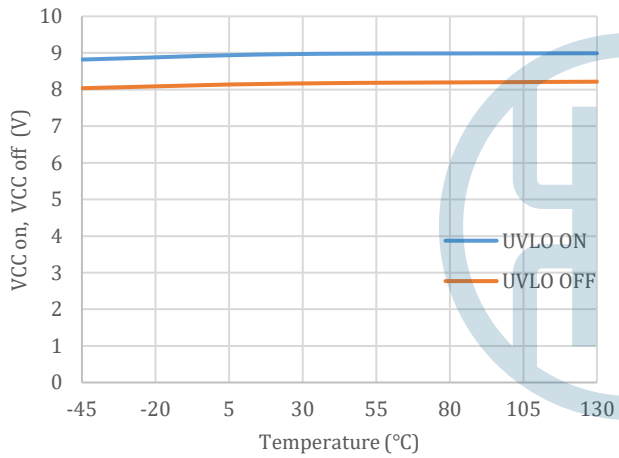


Fig 19. VCC UVLO Thresholds vs Temperature

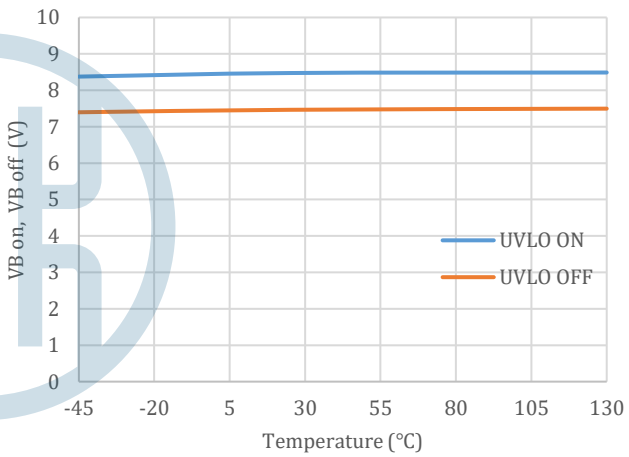


Fig 20. VB-VS UVLO Thresholds vs Temperature

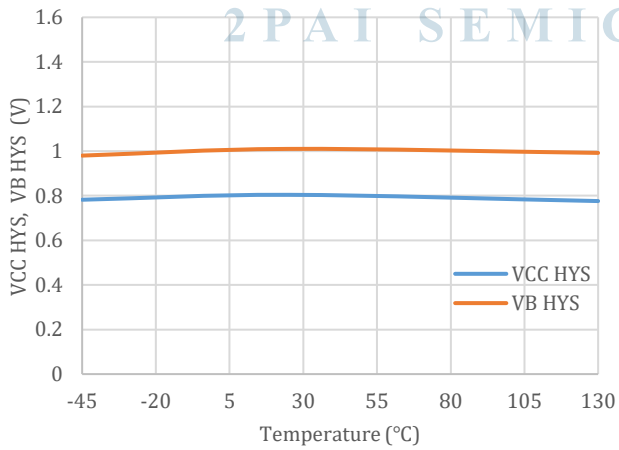


Fig 21. VDD and VHB-VHS UVLO Hysteresis vs Temperature

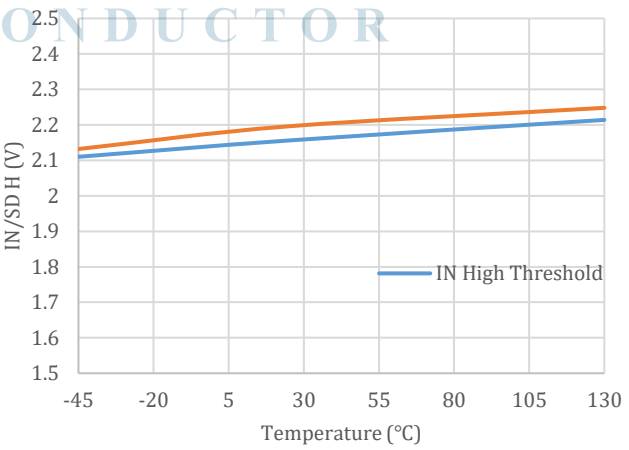


Fig 22. IN/SD Pin High Threshold vs Temperature

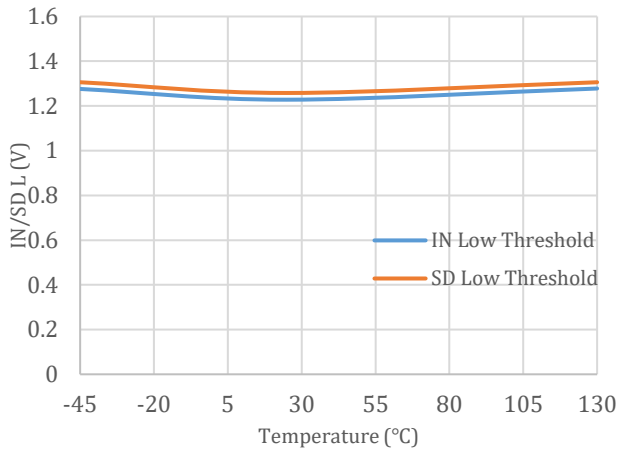


Fig 23. IN/SD Pin Low Threshold vs Temperature

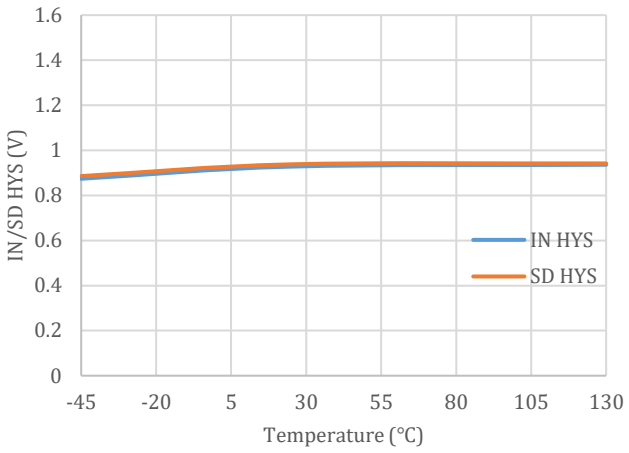


Fig 24. IN/SD Pin Hysteresis vs Temperature

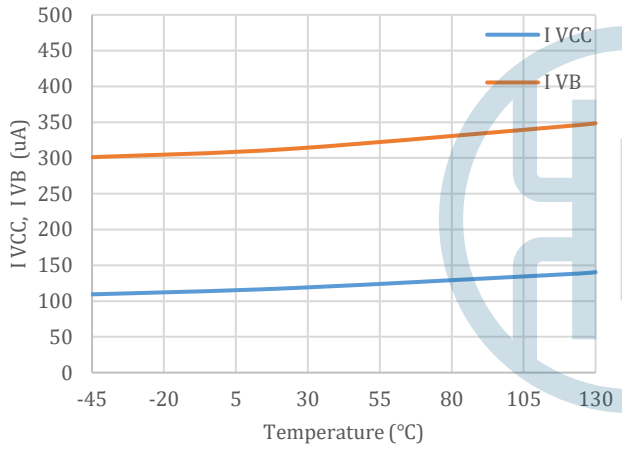


Fig 25. VCC and HB Quiescent Current vs Temperature

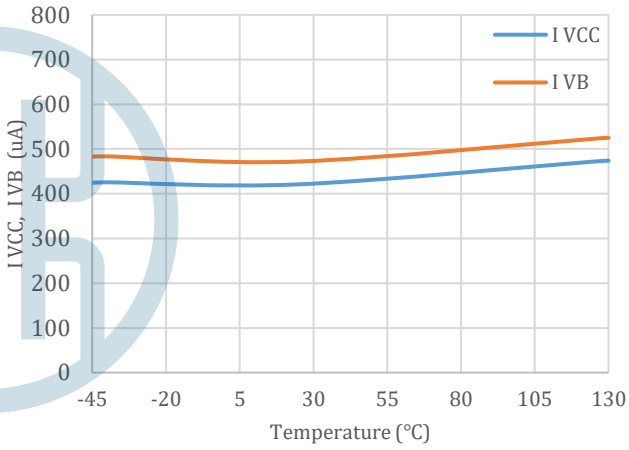


Fig 26. VCC and VB Operating Current vs Temperature

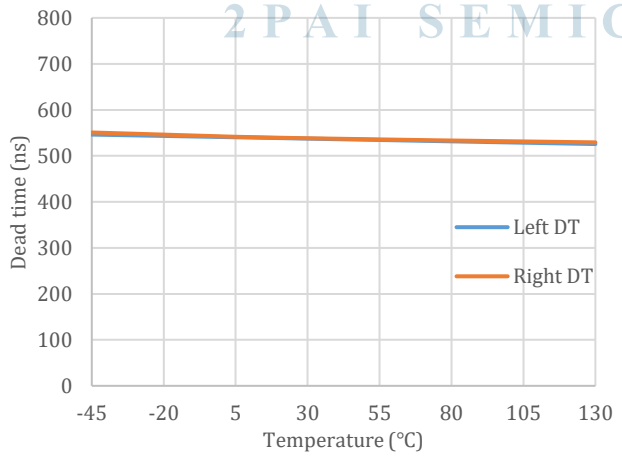


Fig 27. Dead time VS temperature

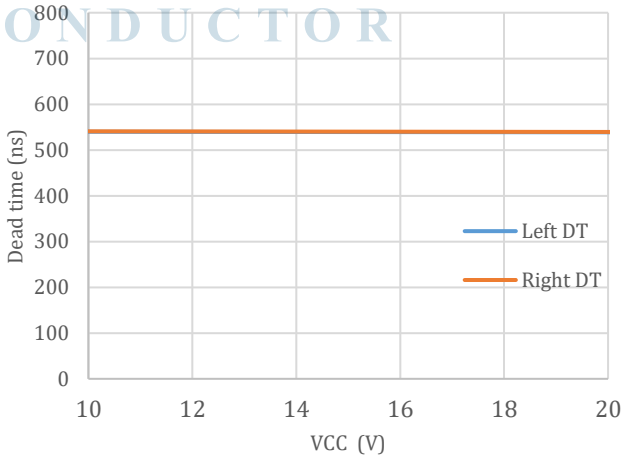


Fig 28. Dead time VS VCC

4. Outline Dimensions

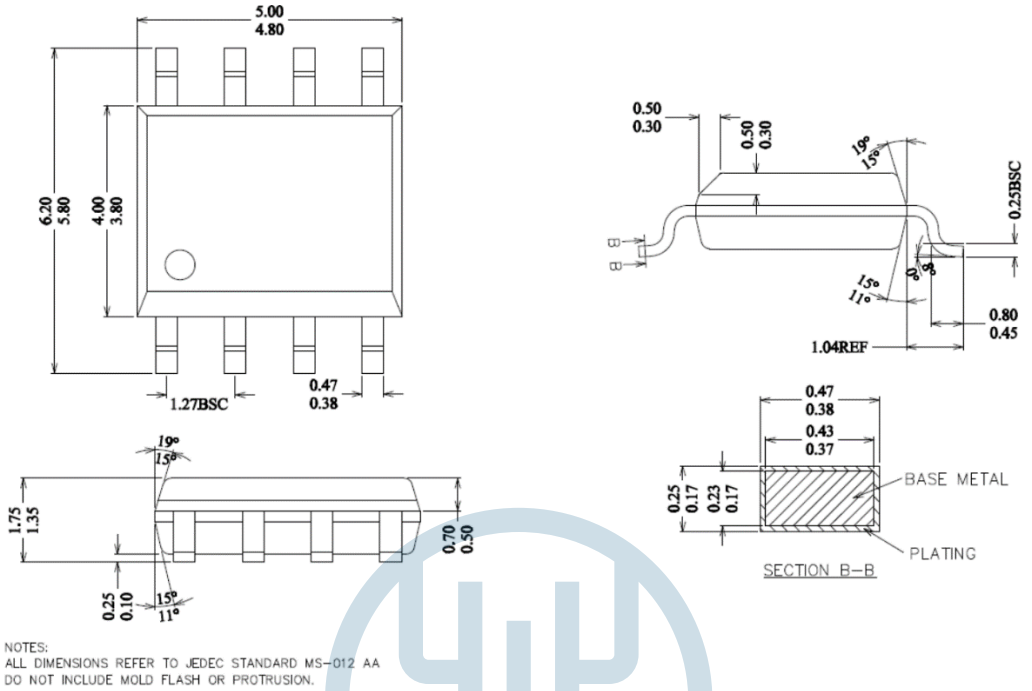


Fig 29. Outline Package

5. Land Patterns

The Fig 30 illustrates the recommended land pattern details for the Pai8171A in a 8-pin Normal body SOIC package. The table lists the values for the dimensions shown in the illustration.

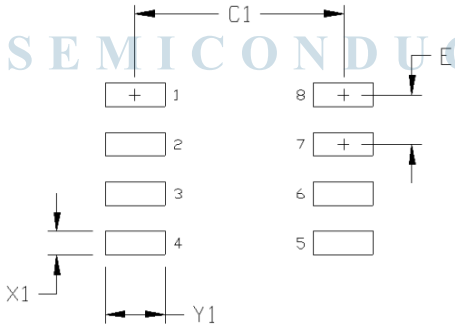


Fig 30. 8-Lead Normal Body SOIC [NB SOIC-8] Land Pattern

8-Lead Normal Body SOIC [NB SOIC-8] Land Pattern Dimensions

DIMENSION	FEATURE	PARAMETER	UNIT
C1	Pad column spacing	5.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.55	mm

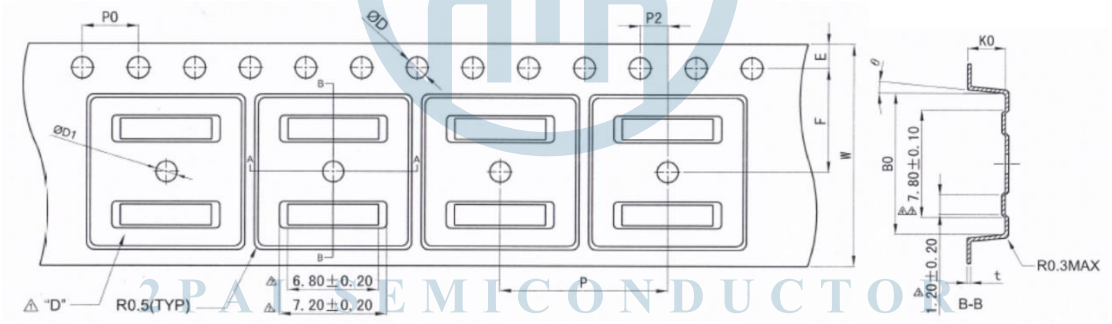
Note：
1.This land pattern design is based on IPC -7351
2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

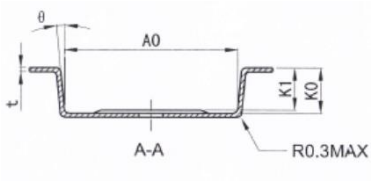
6. Top Marking

Fig 31. Top Marking

Line 1	XXXXXXXX=Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXX, no special meaning

7. Reel Information





Items	Size(mm)
E	1.75±0.10
F	7.50±0.05
P2	2.00±0.05
D	1.55±0.05
D1	1.5±0.10
P0	4.00±0.10
10P0	40.00±0.20

Items	Size(mm)
W	16.00±0.30
P	12.00±0.10
A0	10.90±0.10
B0	10.80±0.10
K0	3.00±0.10
t	0.30±0.05
K1	2.70±0.10
θ	5° TYP

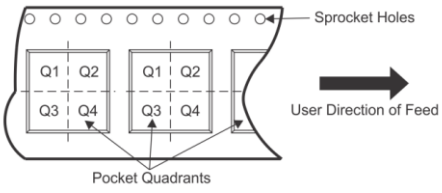


Fig 32. Reel Information

Note：The Pin 1of the chip is in the quadrant Q1

8. Ordering Guide

Ordering Guide

Model Name	Temperature Range	Package	MSL Peak Temp [1]	Quantity per reel
Pai8171A-SR	−40~125°C	NB SOIC-8	Level-2-260℃	2500

Note：

1. MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

9. Important Notice And Disclaimer

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http://www.rpsemi.com/

10. Revision History

Ver	Date	Page	Change Record
0.1	2021-10-25	All	Initial version
0.2	2022-10-10	All	Update All page (Initial release)